


# LCFC Confidential

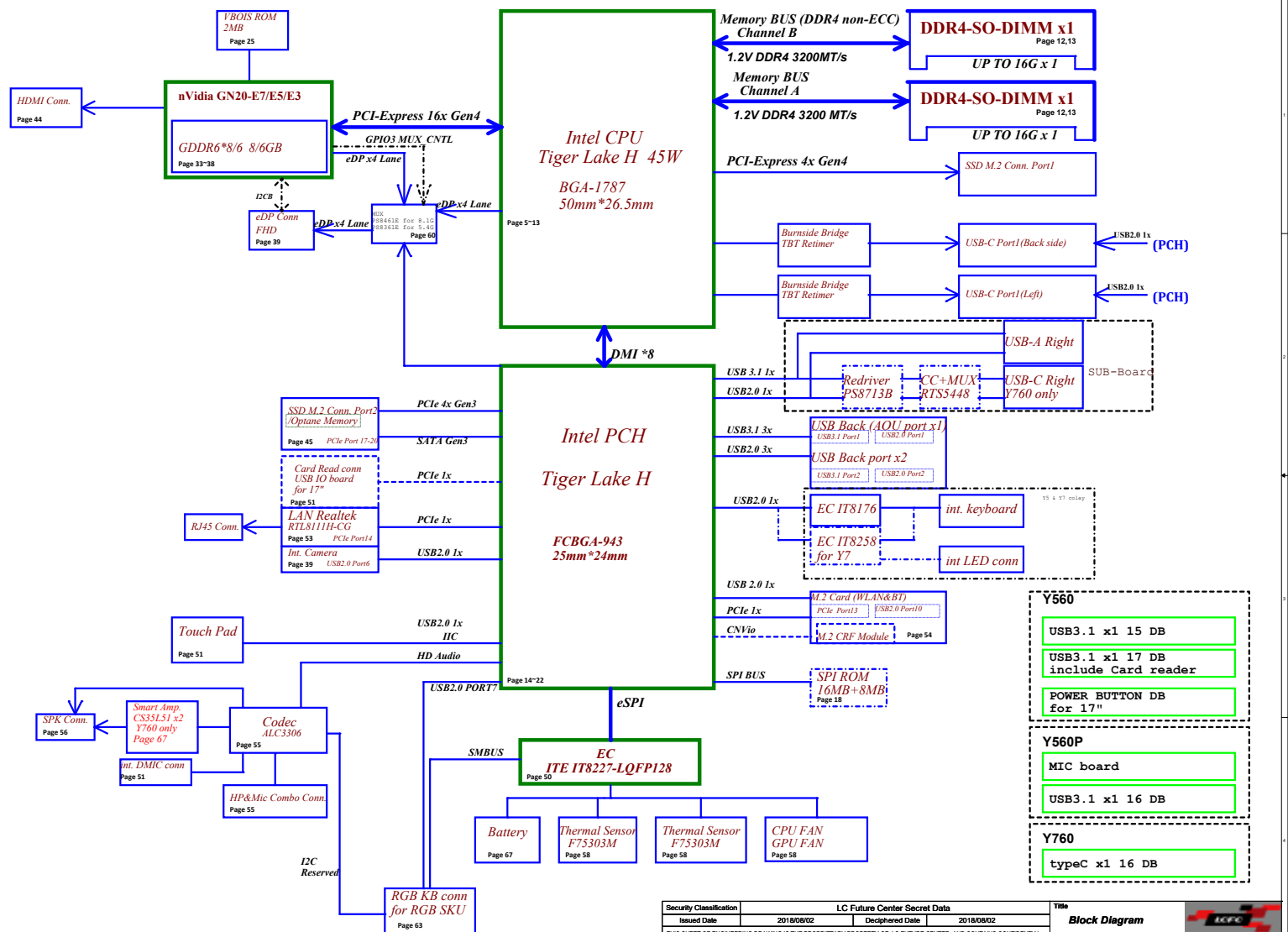
## Y560 M/B Schematics Document

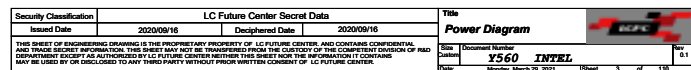
Tiger Lake H-Processor with DDR4 + NV GN20-E GPU

2020-10-10

REV: 0.1

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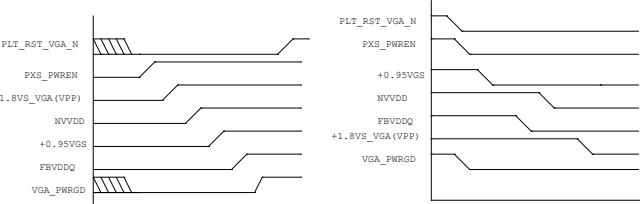




GN20x-E GPIO

GPIO	I/O	GPIO Name	Function Description	Net name	I/O Termination
GPIO0	OUT	NVDDO_PWM_VID	PWM Output to control NVDD	NVDDO_PWM_VID	
GPIO1	OUT	GC6:GC6_FB_EN	FB Enable for GC6	FB_GC6_EN	(10K PD)
GPIO2	IN	GC6:GPU_EVENT*	Wake the GPU from GC6 state	GPU_EVENT#_R	(10K PU)
GPIO3	OUT	DISP_MUX_CNTL	Display MUX control signal	GPU_MUX_CNTL	(10K PD)
GPIO4	OUT	MSVDD_EN	GPU power sequencing for GC6 ---MSVDD_EN	GPIO4_GC6_MSVDD_EN	(10K PU)
GPIO5	OUT	FRAME_LOCK*	Active low Frame Lock for NVSR panel	UNUSED	
GPIO6	OUT	NVDDO_PSI*	Phase Shedding, NVDDO_PSI	NVDDO_PSI	(10K PU) <b>RSVD</b>
GPIO7	OUT	LCD_BL_PWM	LCD Panel Backlight PWM	GPU_EDP_PWM	(100K PD)
GPIO8	OUT	MEM_VDD_CTL	Memory voltage Control	FBVDDQ_SEL	(10K PD)
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert	VGA_ALERT#	(10K PU)
GPIO10	OUT	MEM_VREF_CTL	Memory VREF Control	MEM_VREF_CTL	(100K PD)
GPIO11	OUT	LCD_VDD	LED Panel power enable	GPU_EDP_ENVDD	(10K PD)
GPIO12	IN	PWR_LEVEL	AC power detect or power supply overdraw input	VGA_AC_DET_R	(10K PU)
GPIO13	IN	IGPU_BL_EN	Signal indicating when the IGPU has EN the BL	iGPU_EDP_ENBK	(100K PU)
GPIO14	IN	HPD_IFPA*	Hot Plug Detect for IFPA	IFPA_HPD	(10K PU)
GPIO15	IN	HPD_IFPB*	Hot Plug Detect for IFPB	IFPB_HPD	(10K PU)
GPIO16	OUT	DISP_MUX_PWM_CNTL	Allows switching the PWM between IGPU & DGPU	PWM_SW_SELECT	(10K PD)
GPIO17	IN	HPD_IFPD*	Hot Plug Detect for IFPD	GPU_EDP_HPD	(10K PU)
GPIO18	IN	HPD_IFPE*	Hot Plug Detect for IFPE	UNUSED	
GPIO19	OUT	UNUSED			
GPIO20	OUT	UNUSED			
GPIO21	OUT	LCD_BLEN	LCD Panel Backlight Enable	GPU_EDP_ENBK	(100K PD)
GPIO22	OUT	ADC_MUX_SEL	OVRR MUX Input SEL	ADC_MUX_SEL	(2.2K PU)
GPIO23	OUT	UNUSED			
GPIO24	IN	HPD_IFPF*/USBC_HPD* or DOONLE_DET*	Hot Plug Detect for IFPF or USBC	UNUSED	
GPIO25	OUT	FBVDDO_PSI	Turns off phases of the Frame buffer power supply	FBVDDQ_PSI	(5.1K PU)
GPIO26	OUT	ROM_WP* FP_FUSE	Connect to WP pin of the GPU EEPROM N18P-G61-A Control FP_FUSE	GPIO26_ROM_WP	(10K PD)
GPIO27	IN	HPD_IFPC*	Hot Plug Detect for IFPC	IFPC_HPD	(10K PU)
GPIO28	OUT	MSVDDO_PWM_VID	PWM Outout to CNTL MSVDD	UNUSED	
GPIO29	OUT	NVDDO_EN	NVDDO Enable <b>RSVD</b>	GPIO29_NVDDO_EN	(100K PU) <b>RSVD</b>
GPIO30	OUT	MSVDDO_PSI*	Phase Shedding	UNUSED	

GN20x-E Power Sequence



1. The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
2. It is recommended that the delay from IVB on to PEXDDO/DPD\_PEXDDO assertion not exceed 10ms.
3. The ramp-up overshoot should not exceed the silicon reliability limit voltage.
4. Power up NVDDO must be 90% before PEXDDO can ramp-up.
5. Refer to the JEDEC Memory SP9C for memory-related power sequencing.
7. FBVDDQ, USB\_VDDP and IVB\_AON don't need power cycle for GC6

1. For G2026, VPP must be equal to or higher than FBVDDQ at all times; use gate logic and discharge circuit as needed.
2. All 3.3V devices that connect to the GPU must be ramp down before IVB; GPU can NOT have any 3.3V leakage path after IVB power down.
3. Power down of PEXDDO must be less than 10% before NVDDO can start ramp-down.

H=High: Tied to 1.8V  
M=Middle: Tied to 0.9V  
L=Low: Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	GN20x-E VRAM
L	L	L	0 (0x0000)	Samsung K4J280325BC-HC14
L	L	H	1 (0x0001)	Micron MT61K256M32JE-14-A
L	H	L	2 (0x0002)	Hynix H56C8H24AIR-S2C
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	Samsung(or E7) K4ZAF3259M-HC 14
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

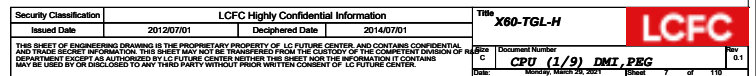
FS\_OVR# FUNCTION

ROM_SO	ROM_SI	ROM_SCLK	FS_OVR# FUNCTION
L	L	H	FS_OVR# function ENABLE
L	L	L	FS_OVR# function DISABLED Reserved; do not configure

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	0
L	L	L	0	0	0	0

- 1:SMB\_ALT\_ADDR ENABLE
- 0:SMB\_ALT\_ADDR DISABLE
- 1:DEVID\_SEL REBRAND
- 0:DEVID\_SEL ORIGINAL
- 1:PCIE\_CFG LOW POWER
- 0:PCIE\_CFG HIGH POWER
- 1:VGA\_DEVICE ENABLE
- 0:VGA\_DEVICE DISABLE

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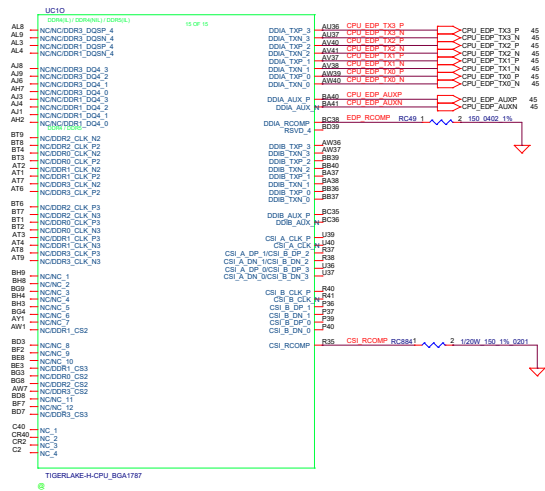








RSVD	
CFG0	N/A
Reserved configuration lane	
CFG1	N/A
PCI Express® Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation ★ 0 = Lane numbers reversed.
Reserved configuration lane	
CFG3	N/A
xDP enable	
CFG4	1 = Disabled. ★ 0 = Enabled.
PCI Express® Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express® 01 = reserved 10 = 2 x8 PCI Express® ★ 11 = 1 x16 PCI Express®
Reserved configuration lane	
CFG[13:7]	N/A
PCIe4 LANE reversal	
CFG14	★ 1 = (default) normal 0 = Reversed

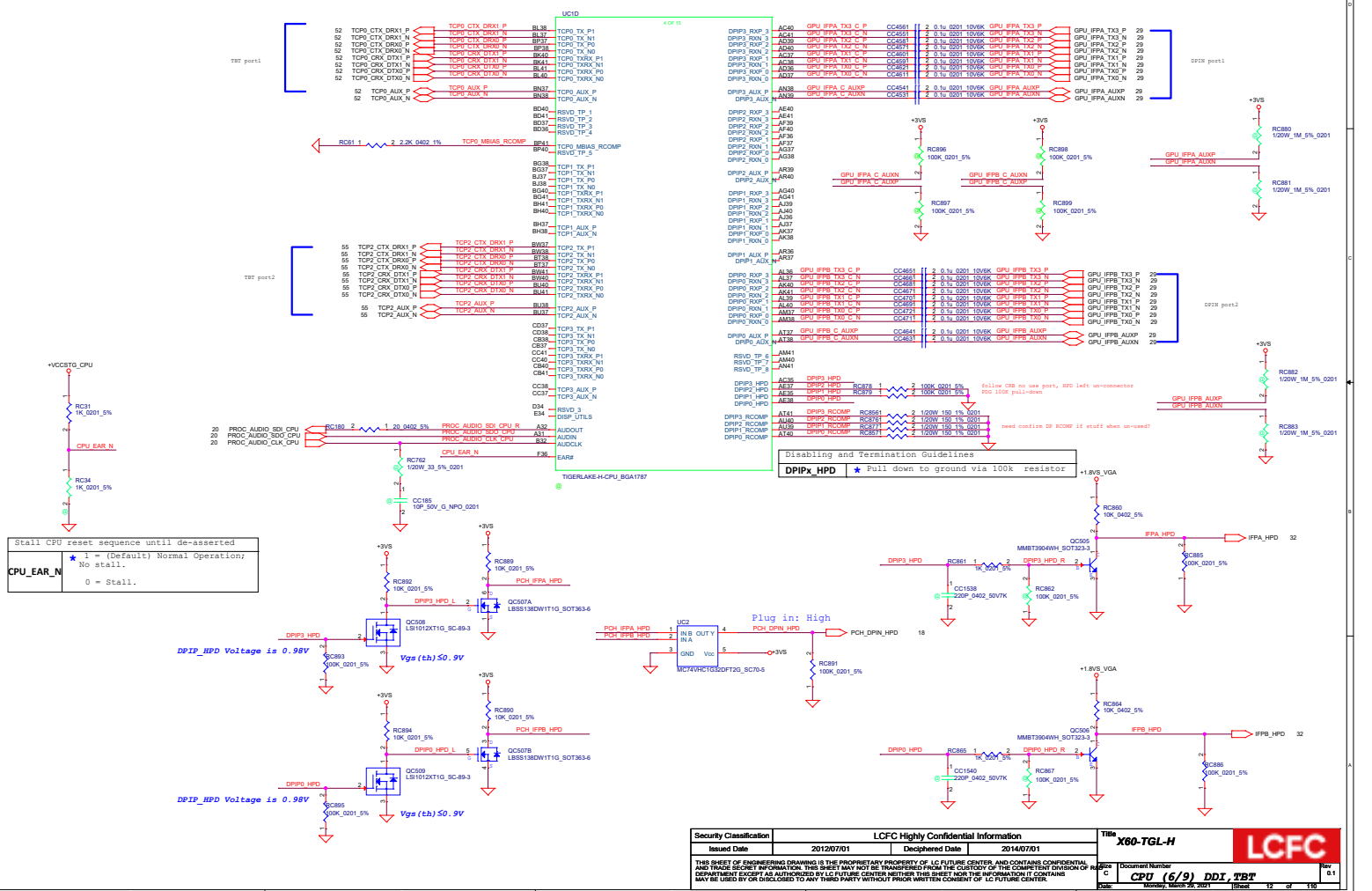
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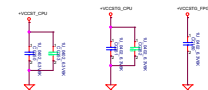
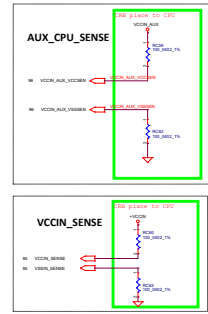
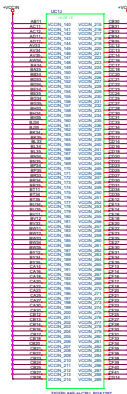


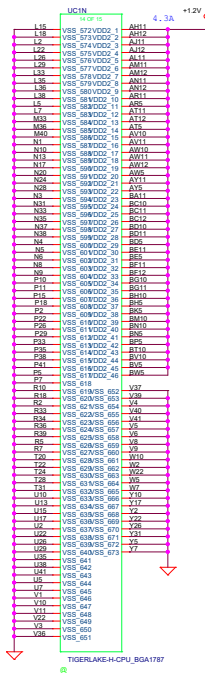
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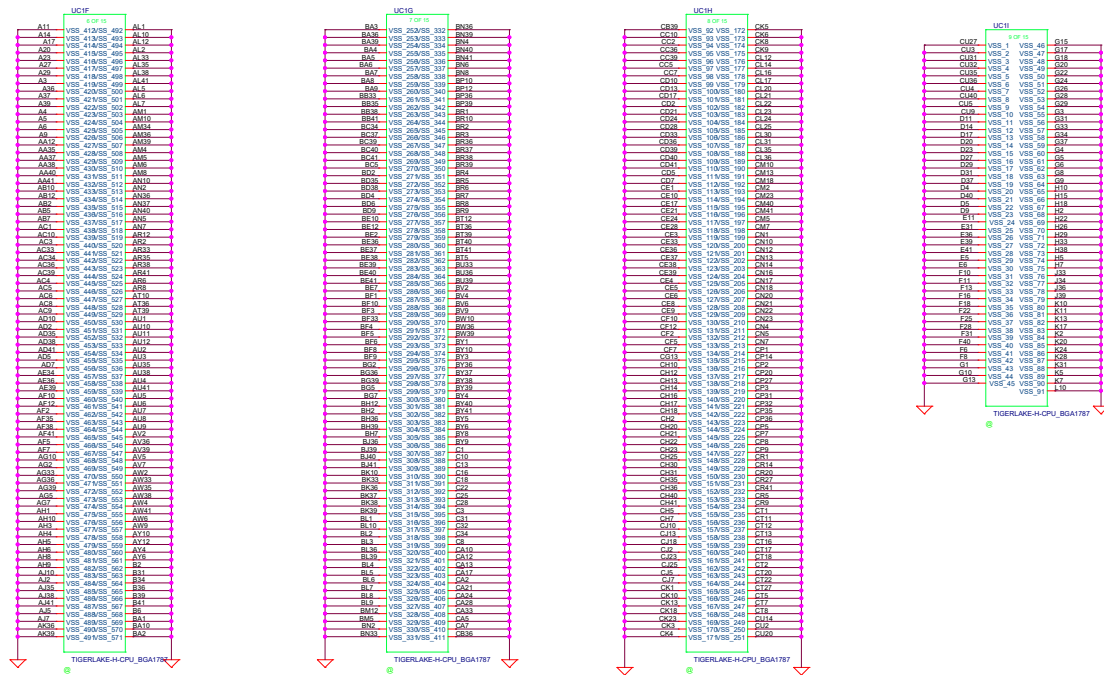
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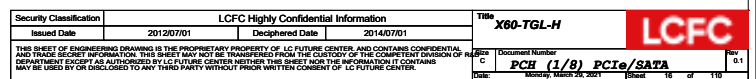


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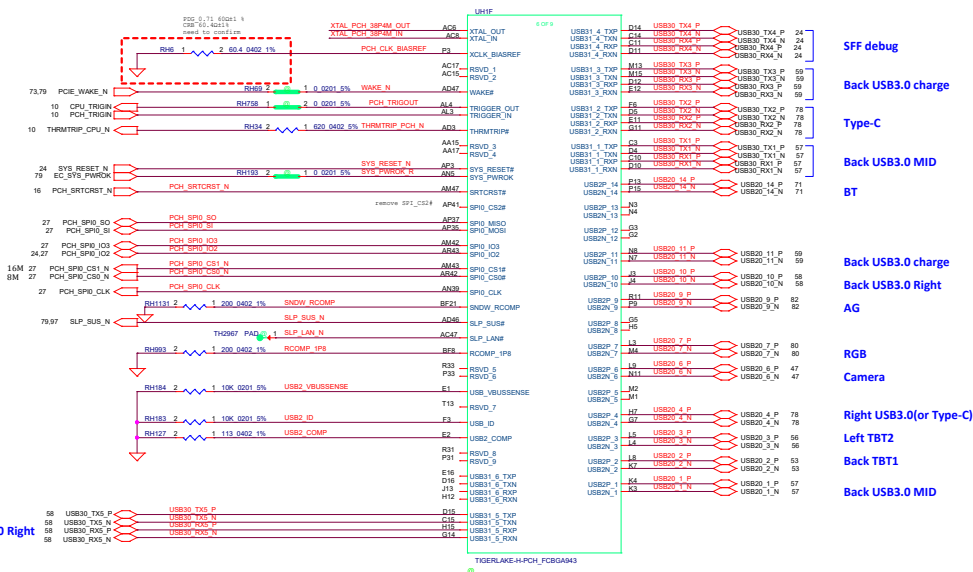
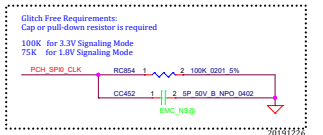
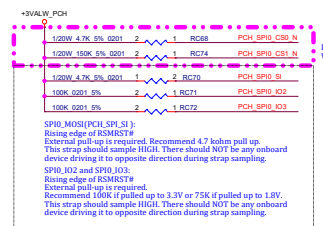
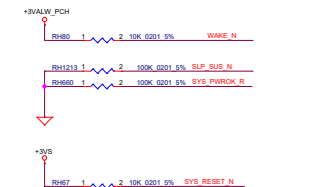
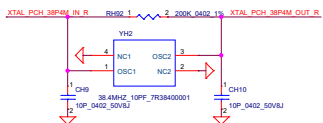


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EXC24CH500U\_4P

LC5

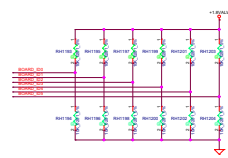
XTAL\_PCH\_38P4M\_OUT RH32 1 20 0.402 5% XTAL\_PCH\_38P4M\_OUT\_R




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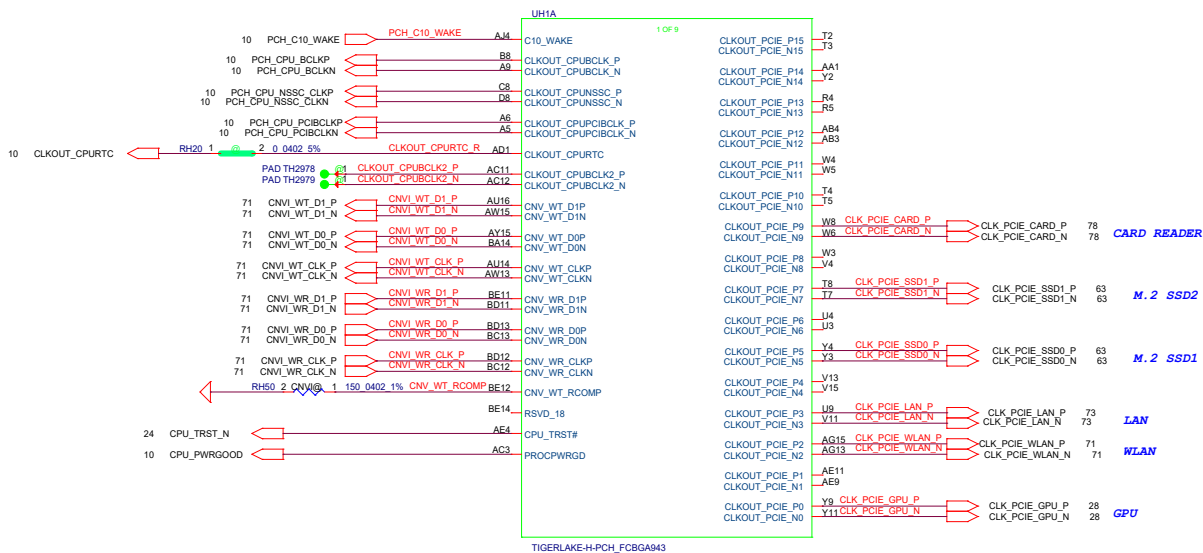




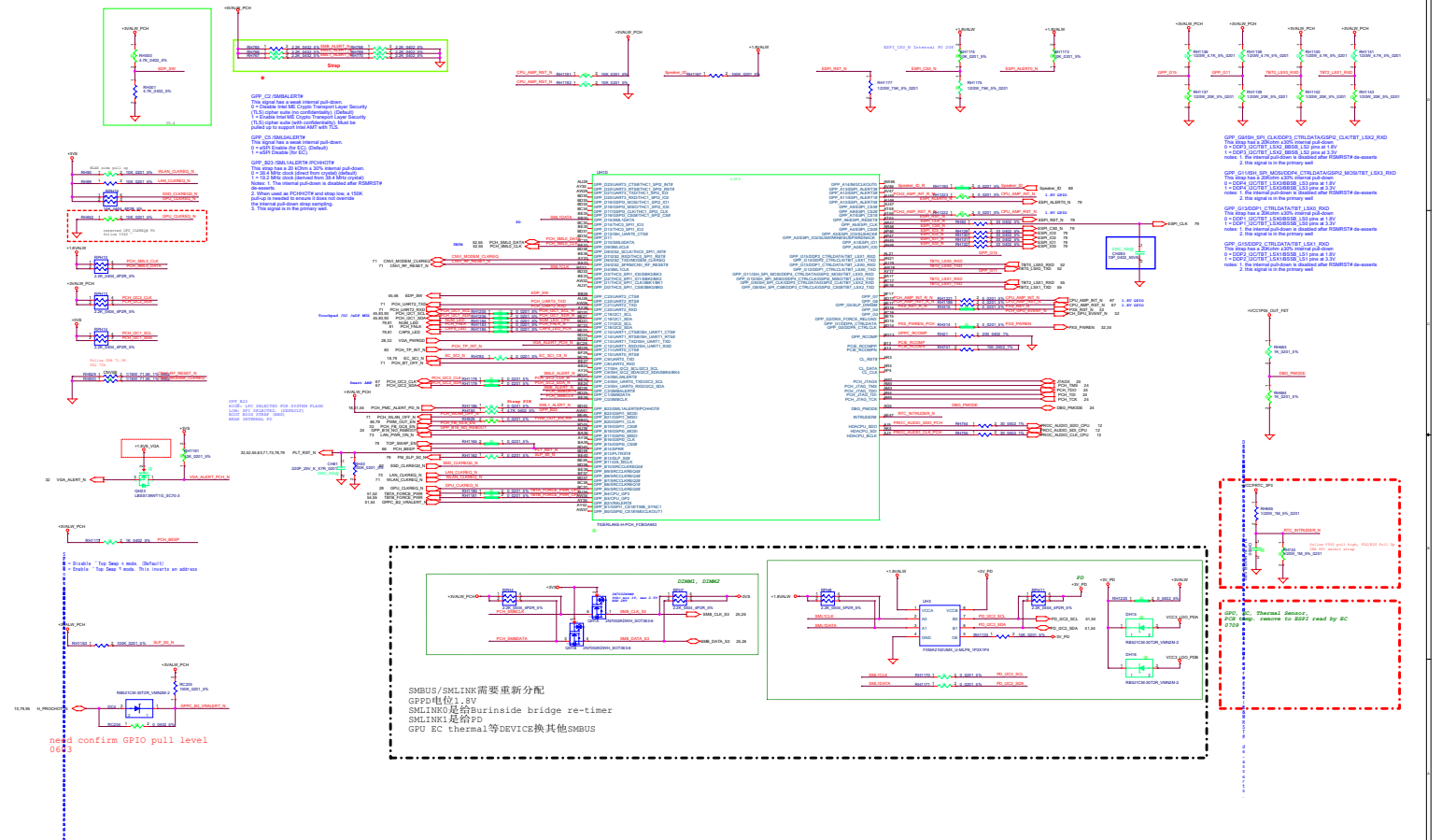
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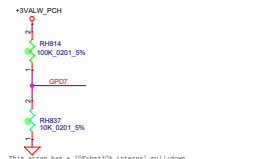
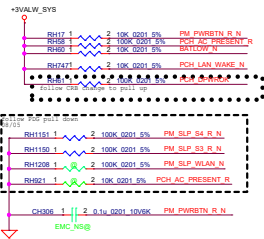
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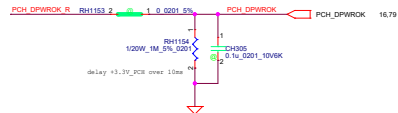
SMBUS/SMLINK需要重新分配  
GPPD电压1.2V  
SMLINK是桥burinside bridge re-timer  
SMLINK1是给PD  
GPU SC thermal等DEVICE换其他SMBUS



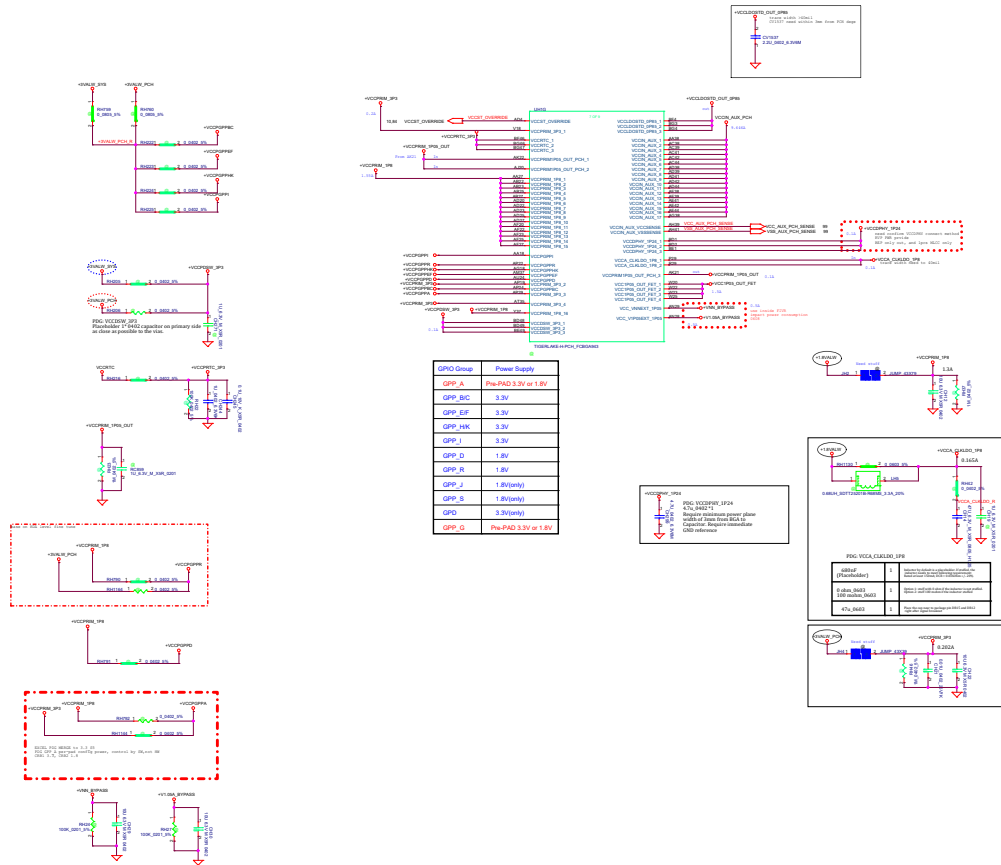
This strap has a 200kOhm internal pull-down  
This strap should sample 120V. There should  
not be any on-board device driving it to opposite direction  
during strap sampling.  
NOTES: 1. The internal pull-down is disabled after  
DSW\_RESET is high  
2. This signal is in the DSW well.



DSWROK can be tied to RDMSTN for platforms  
that does not support the DSW in state.



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191H		
E of S		F of S
A17	VSS 163/SS 240	A23
A18	VSS 164/SS 241	A24
A19	VSS 165/SS 242	A25
A20	VSS 166/SS 243	A26
A21	VSS 167/SS 244	A27
A22	VSS 168/SS 245	A28
A23	VSS 169/SS 246	A29
A24	VSS 170/SS 247	A30
A25	VSS 171/SS 248	A31
A26	VSS 172/SS 249	A32
A27	VSS 173/SS 250	A33
A28	VSS 174/SS 251	A34
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A37	VSS 183/SS 260	A43
A38	VSS 184/SS 261	A44
A39	VSS 185/SS 262	A45
A40	VSS 186/SS 263	A46
A41	VSS 187/SS 264	A47
A42	VSS 188/SS 265	A48
A43	VSS 189/SS 266	A49
A44	VSS 190/SS 267	A50
A45	VSS 191/SS 268	A51
A46	VSS 192/SS 269	A52
A47	VSS 193/SS 270	A53
A48	VSS 194/SS 271	A54
A49	VSS 195/SS 272	A55
A50	VSS 196/SS 273	A56
A51	VSS 197/SS 274	A57
A52	VSS 198/SS 275	A58
A53	VSS 199/SS 276	A59
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A88	VSS 234/SS 311	A94
A89	VSS 235/SS 312	A95
A90	VSS 236/SS 313	A96
A91	VSS 237/SS 314	A97
A92	VSS 238/SS 315	A98
A93	VSS 239/SS 316	A99

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191H		
E of S		F of S
A100	VSS 1	VSS 78
A101	VSS 2	VSS 79
A102	VSS 3	VSS 80
A103	VSS 4	VSS 81
A104	VSS 5	VSS 82
A105	VSS 6	VSS 83
A106	VSS 7	VSS 84
A107	VSS 8	VSS 85
A108	VSS 9	VSS 86
A109	VSS 10	VSS 87
A110	VSS 11	VSS 88
A111	VSS 12	VSS 89
A112	VSS 13	VSS 90
A113	VSS 14	VSS 91
A114	VSS 15	VSS 92
A115	VSS 16	VSS 93
A116	VSS 17	VSS 94
A117	VSS 18	VSS 95
A118	VSS 19	VSS 96
A119	VSS 20	VSS 97
A120	VSS 21	VSS 98
A121	VSS 22	VSS 99
A122	VSS 23	VSS 100
A123	VSS 24	VSS 101
A124	VSS 25	VSS 102
A125	VSS 26	VSS 103
A126	VSS 27	VSS 104
A127	VSS 28	VSS 105
A128	VSS 29	VSS 106
A129	VSS 30	VSS 107
A130	VSS 31	VSS 108
A131	VSS 32	VSS 109
A132	VSS 33	VSS 110
A133	VSS 34	VSS 111
A134	VSS 35	VSS 112
A135	VSS 36	VSS 113
A136	VSS 37	VSS 114
A137	VSS 38	VSS 115
A138	VSS 39	VSS 116
A139	VSS 40	VSS 117
A140	VSS 41	VSS 118
A141	VSS 42	VSS 119
A142	VSS 43	VSS 120
A143	VSS 44	VSS 121
A144	VSS 45	VSS 122
A145	VSS 46	VSS 123
A146	VSS 47	VSS 124
A147	VSS 48	VSS 125
A148	VSS 49	VSS 126
A149	VSS 50	VSS 127
A150	VSS 51	VSS 128
A151	VSS 52	VSS 129
A152	VSS 53	VSS 130
A153	VSS 54	VSS 131
A154	VSS 55	VSS 132
A155	VSS 56	VSS 133
A156	VSS 57	VSS 134
A157	VSS 58	VSS 135
A158	VSS 59	VSS 136
A159	VSS 60	VSS 137
A160	VSS 61	VSS 138
A161	VSS 62	VSS 139
A162	VSS 63	VSS 140
A163	VSS 64	VSS 141
A164	VSS 65	VSS 142
A165	VSS 66	VSS 143
A166	VSS 67	VSS 144
A167	VSS 68	VSS 145
A168	VSS 69	VSS 146
A169	VSS 70	VSS 147
A170	VSS 71	VSS 148
A171	VSS 72	VSS 149
A172	VSS 73	VSS 150
A173	VSS 74	VSS 151
A174	VSS 75	VSS 152
A175	VSS 76	VSS 153
A176	VSS 77	VSS 154
A177	VSS 78	VSS 155
A178	VSS 79	VSS 156
A179	VSS 80	VSS 157
A180	VSS 81	VSS 158
A181	VSS 82	VSS 159
A182	VSS 83	VSS 160
A183	VSS 84	VSS 161
A184	VSS 85	VSS 162

TIGERLAKE-H-PCH\_FCB0643

6

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Document Number	PCH (8/8) VSS		Rev
Date	Monday, March 24, 2021	Sheet	23 of 110

TABLE : CPU ITP DEBUG REPORT

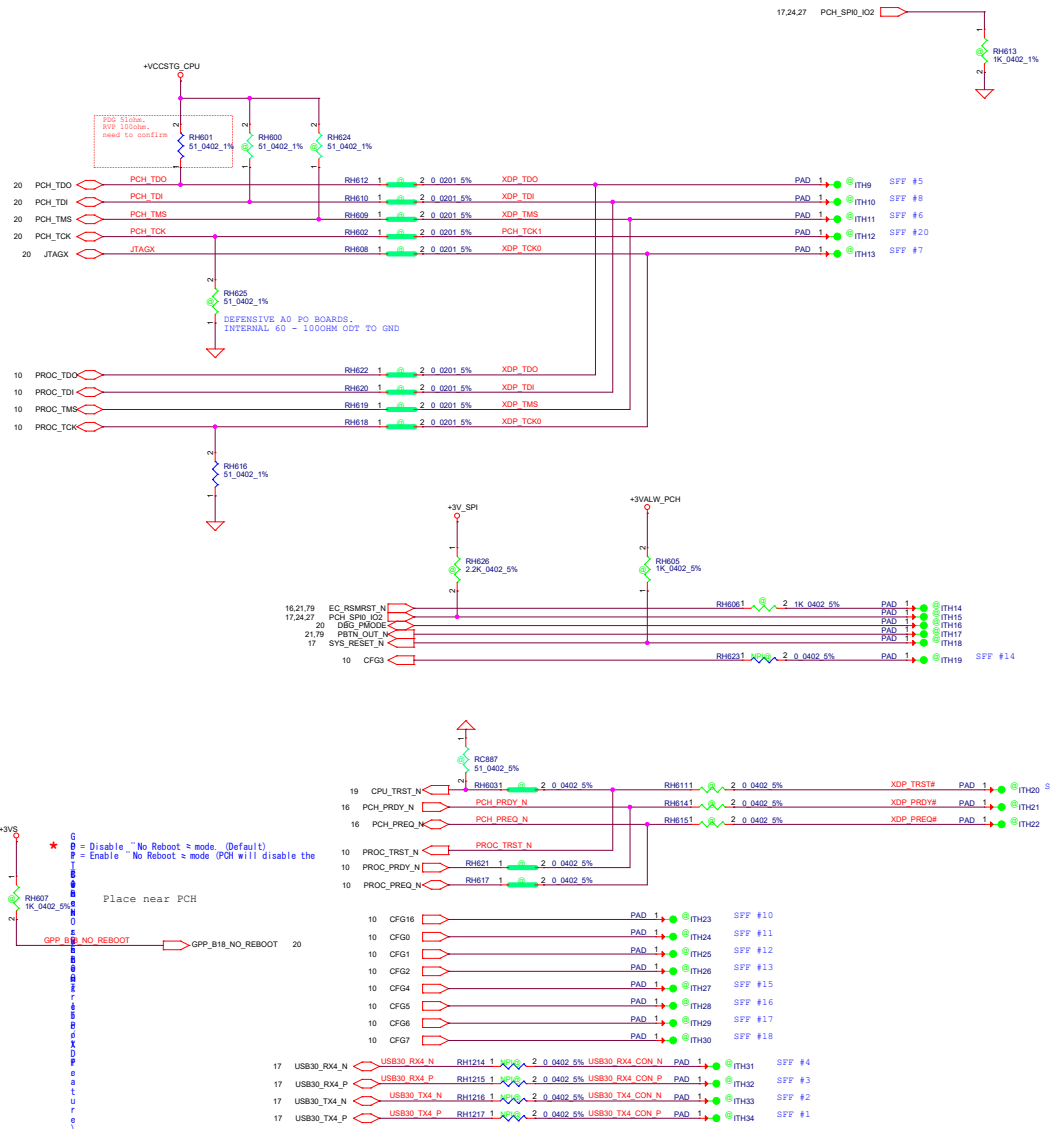
	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

TABLE : PCH ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

TABLE : Functional Strap

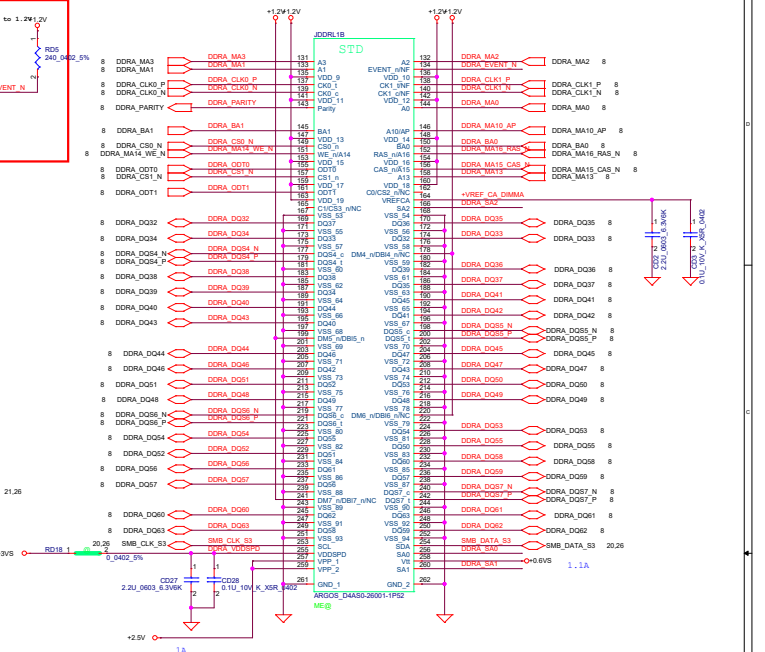
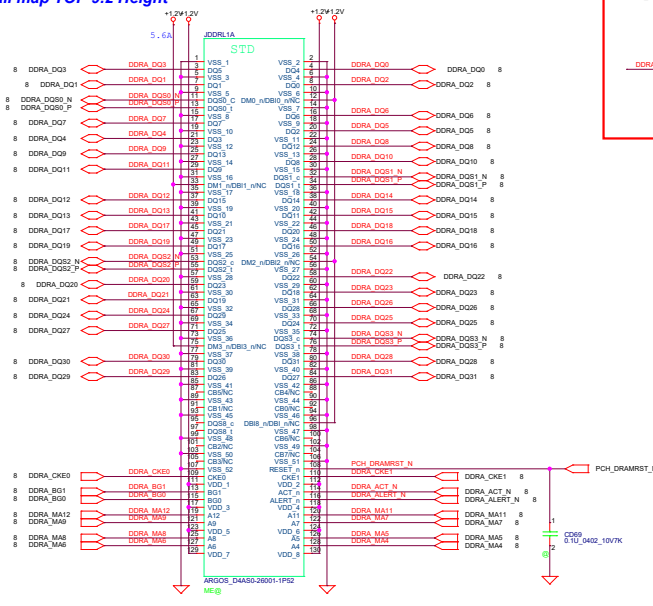
GPP_B18/GSPI0_MOSI (No Reboot)	R563
HIGH Enable "No Reboot" Mode	ASM
LOW Disable "No Reboot" Mode (Default)	NO ASM



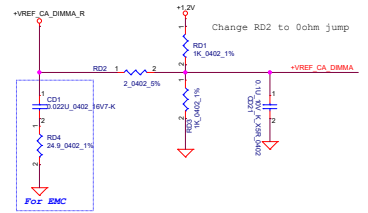
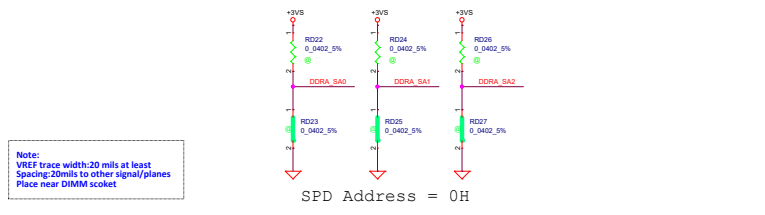
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Issued Date	2018/08/02	Deciphered Date	2018/08/02	XDP			
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Size	Document Number	Rev					
Custom	Y550	0.1					
Date	Monday, March 26, 2021	Sheet	24	of 110			

# DDR4 SO-DIMM

follow CRB ball map TOP 9.2 Height



Note:  
VREF trace width:20 mils at least  
Spacing:20mils to other signal/planes  
Place near DIMM socket

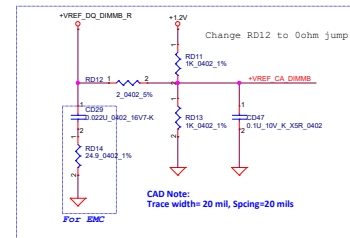
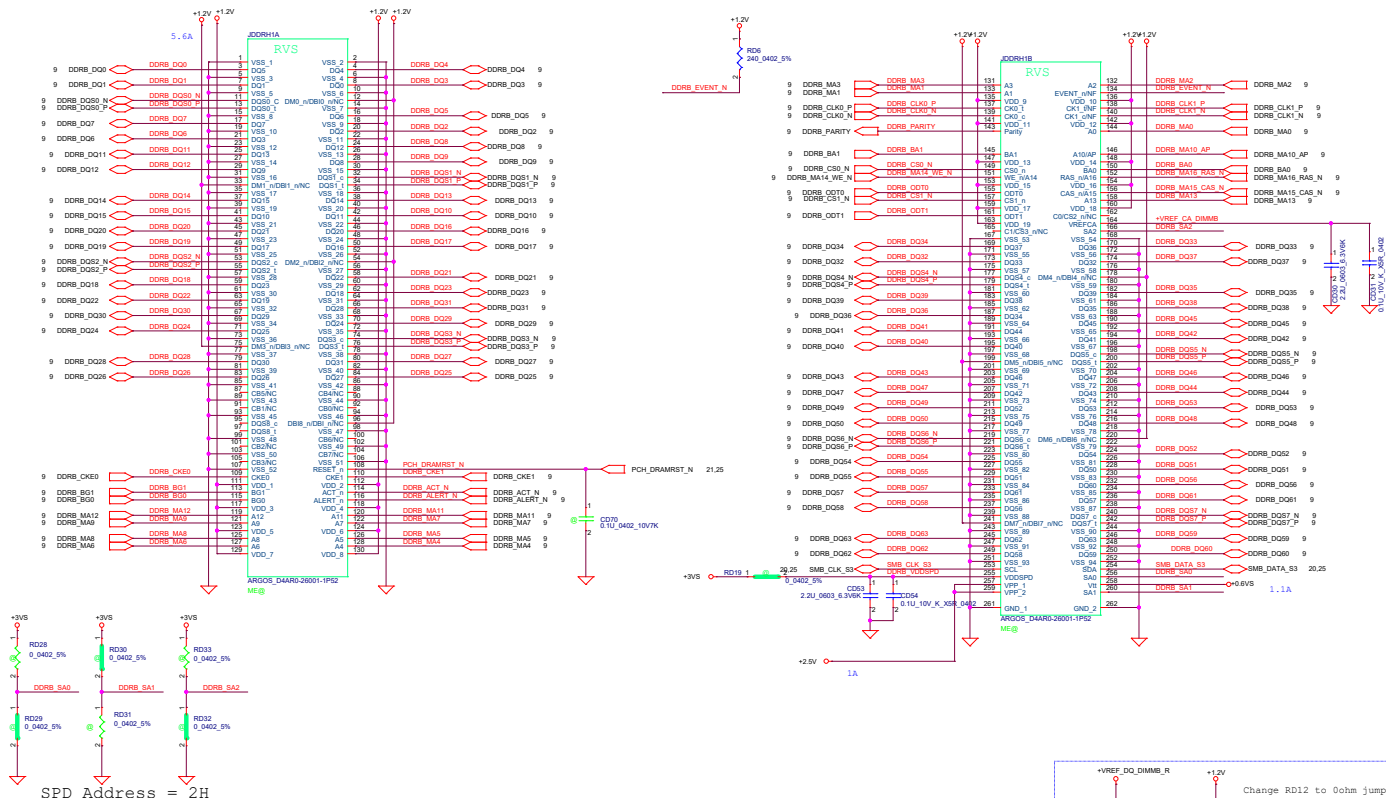


Security Classification				Title	
LC Future Center Secret Data				DDR4 SO-DIMM A	
Issued Date	2018/08/02	Deciphered Date	2018/08/02	Document Number	Y550
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				Sheet	25 of 110

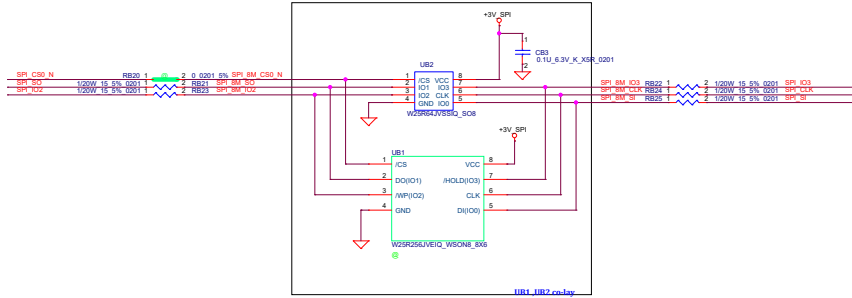
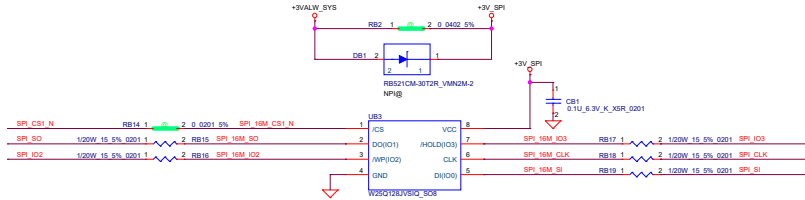
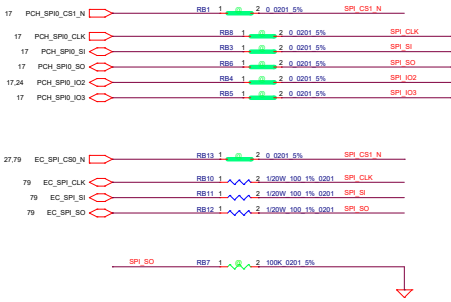


## DDR4 SO-DIMM B

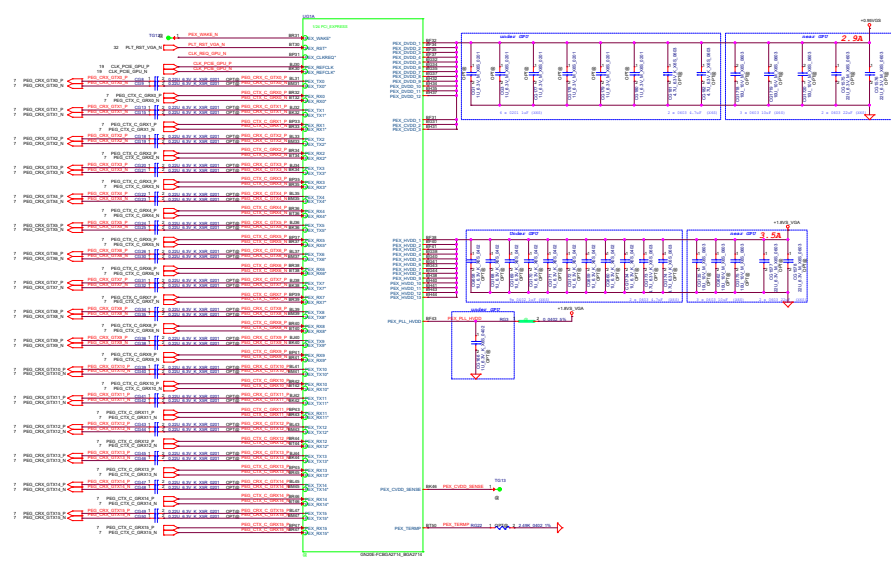
Follow CRB ball map TOP 5.2 Height



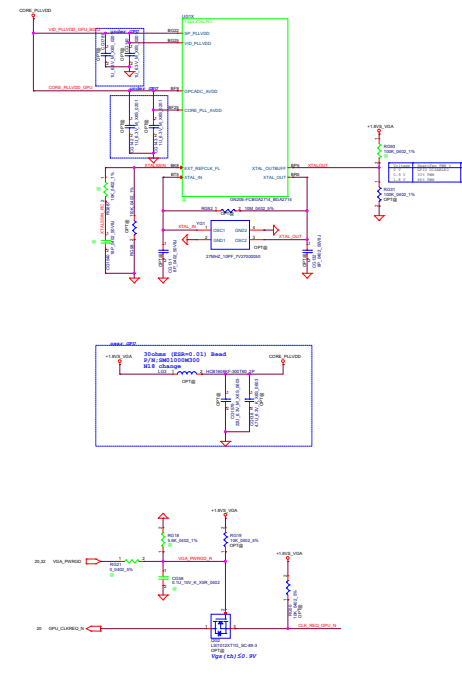
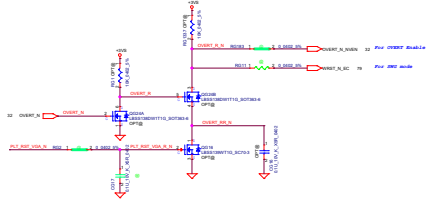
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Issued Date	2018/08/02	Deciphered Date	2018/08/02	Doc No	DDR4 SO-DIMM B
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				Doc No	Y550
				Date	Monday, March 24, 2021
				Sheet	26 of 110



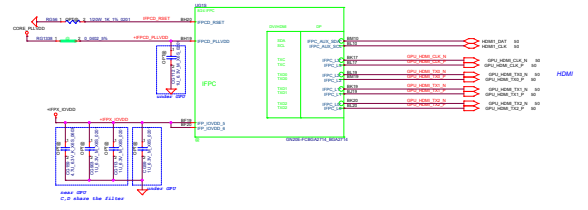
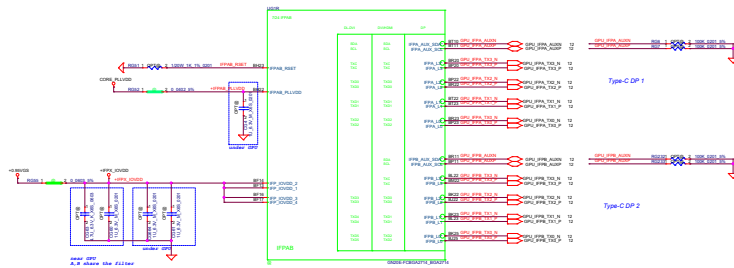
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Issued Date			2012/07/01		Deciphered Date		2014/07/01			
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Doc No		C		Document Number		SPI ROM/TPM			Rev	0.1
Date		Monday, March 24, 2014				Sheet		27	of	110



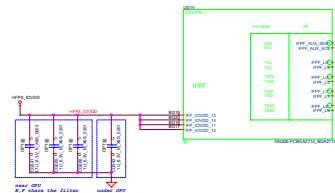
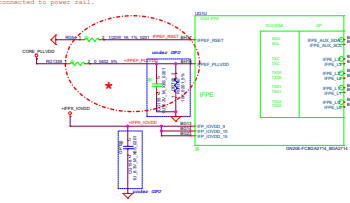
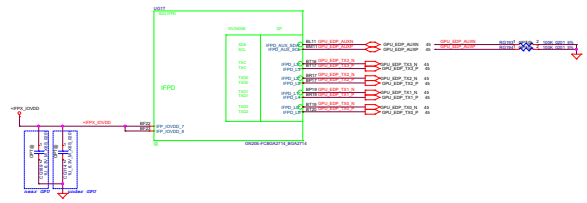
### FS\_OVERT# FUNCTION



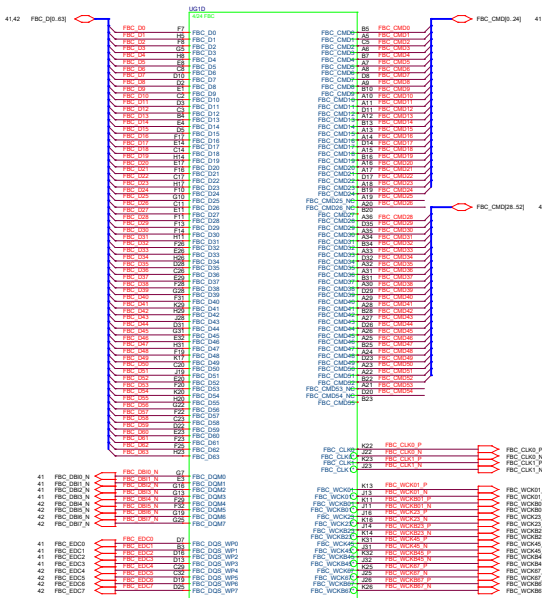
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Revised Date	20180402	Dissemination Date	20180402	HW-01_PSD-IP
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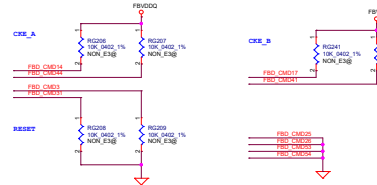
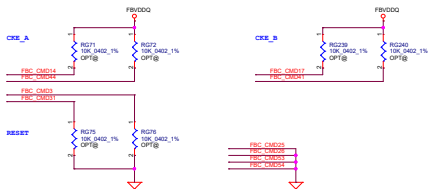
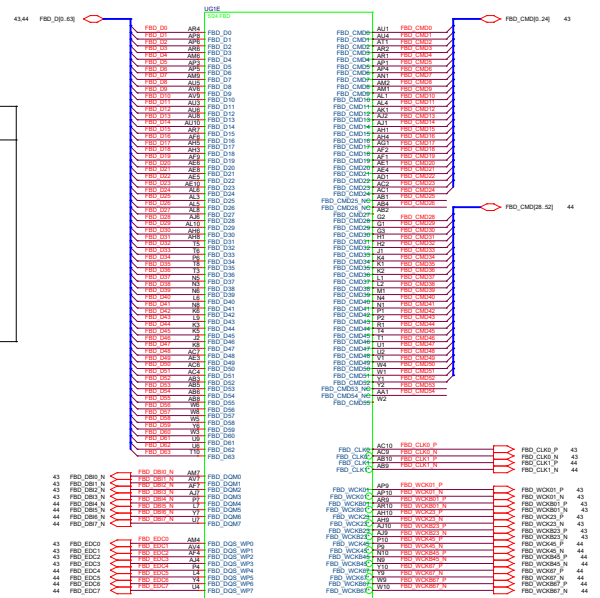
1. If an IFF link is unused, The main and AUX links, IFFray\_MSTP can be left unconnected, and IFFray\_FullVDD should be left to GND.
2. IFF\_FullVDD rail can be left unconnected if no IFF link is used. If any IFF is used, all IFF\_FullVDD rails must be connected to power rail.

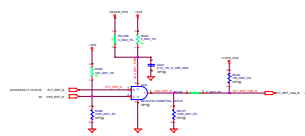
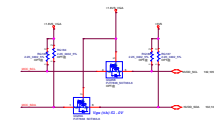
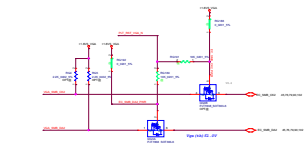
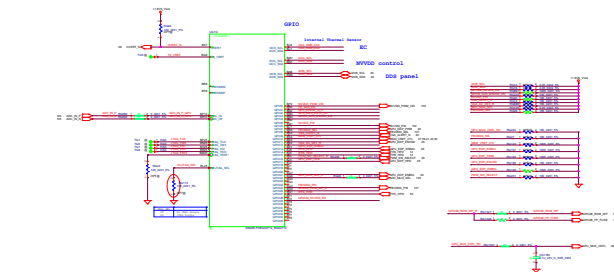




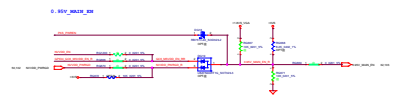
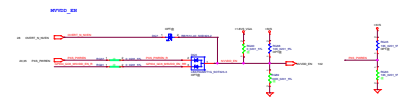


Signal Name (Pin)		Signal Name (Pin)
41	FBC_CMD0	FBC_CMD0
42	FBC_CMD1	FBC_CMD1
43	FBC_CMD2	FBC_CMD2
44	FBC_CMD3	FBC_CMD3
45	FBC_CMD4	FBC_CMD4
46	FBC_CMD5	FBC_CMD5
47	FBC_CMD6	FBC_CMD6
48	FBC_CMD7	FBC_CMD7
49	FBC_CMD8	FBC_CMD8
50	FBC_CMD9	FBC_CMD9
51	FBC_CMD10	FBC_CMD10
52	FBC_CMD11	FBC_CMD11
53	FBC_CMD12	FBC_CMD12
54	FBC_CMD13	FBC_CMD13
55	FBC_CMD14	FBC_CMD14
56	FBC_CMD15	FBC_CMD15
57	FBC_CMD16	FBC_CMD16
58	FBC_CMD17	FBC_CMD17
59	FBC_CMD18	FBC_CMD18
60	FBC_CMD19	FBC_CMD19
61	FBC_CMD20	FBC_CMD20
62	FBC_CMD21	FBC_CMD21
63	FBC_CMD22	FBC_CMD22
64	FBC_CMD23	FBC_CMD23
65	FBC_CMD24	FBC_CMD24
66	FBC_CMD25	FBC_CMD25
67	FBC_CMD26	FBC_CMD26
68	FBC_CMD27	FBC_CMD27
69	FBC_CMD28	FBC_CMD28
70	FBC_CMD29	FBC_CMD29
71	FBC_CMD30	FBC_CMD30
72	FBC_CMD31	FBC_CMD31
73	FBC_CMD32	FBC_CMD32
74	FBC_CMD33	FBC_CMD33
75	FBC_CMD34	FBC_CMD34
76	FBC_CMD35	FBC_CMD35
77	FBC_CMD36	FBC_CMD36
78	FBC_CMD37	FBC_CMD37
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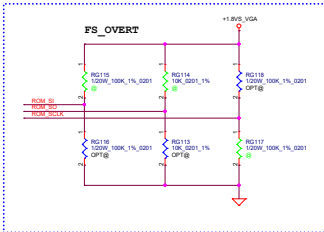
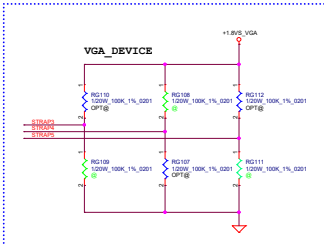
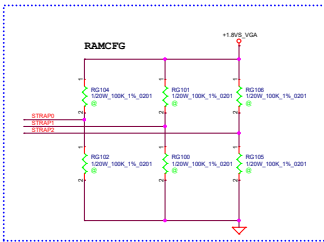
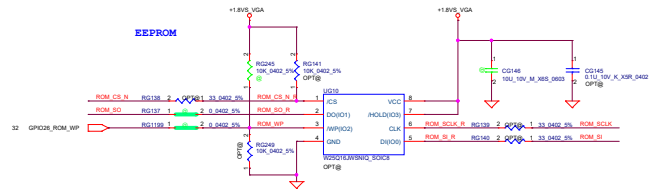
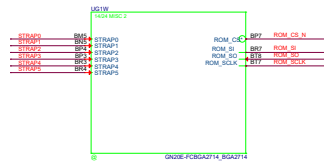


# Power on/off sequence



# Discharge





#### VRAMCFG

GPU VRAM	FS Memory (GDDR6)	RAMCFG[2:0]	STRAP2	STRAP1	STRAP0
GN20a-E7	Samsung 8Gb	E42B0325BC-BC14	0 (0x0000)	L	L
GN20a-E5	Micron 8Gb	MT61K256K32B-14:A	1 (0x0001)	L	H
GN20a-E4	Hynix 8Gb	H56CSH24LR-S2C	2 (0x0002)	L	L
GN20a-E3	Samsung 16Gb	R42AF3258B-BC 14	9 (0x0009)	L	L

#### VGA\_DEVICE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	H	0	0	0	1

0:DEVID\_SEL for Non G-SYNC SKU

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
H	L	H	0	1	0	1

1:DEVID\_SEL for G-SYNC SKU

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL  
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE

#### FS\_OVERT

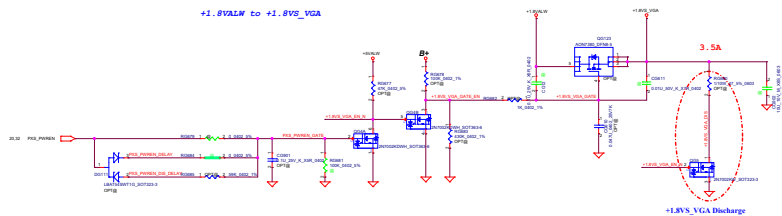
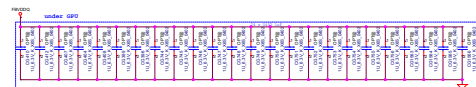
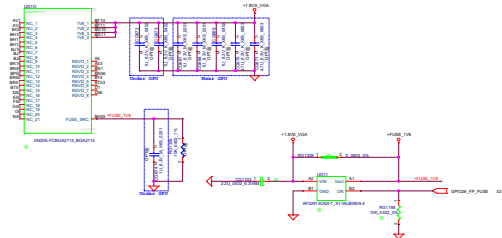
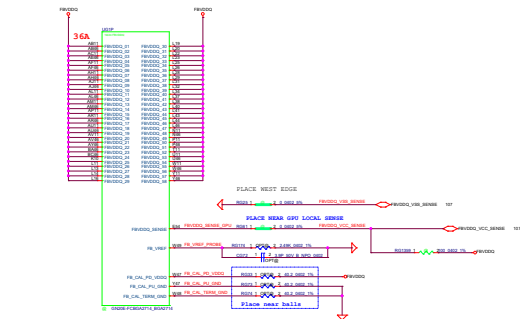
GPU	ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT
GN20x	L	L	H	ENABLE

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Issued Date	2018/08/02	Declassify Date	2018/08/02
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Date			Monday, March 26, 2021 10:04:35 AM of 118

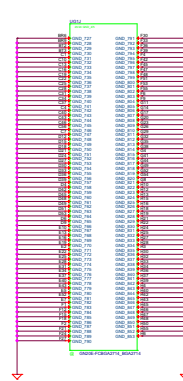
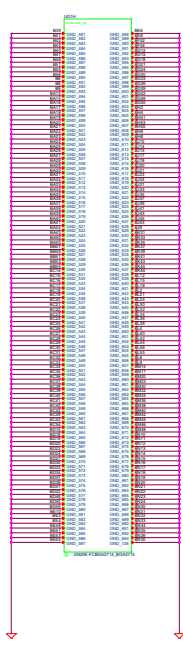
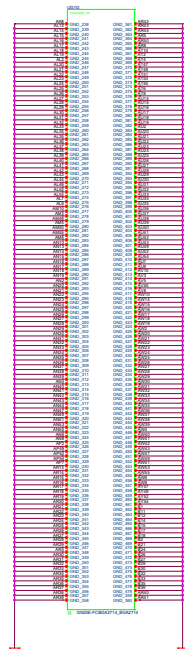
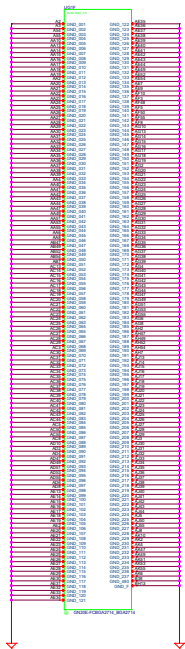
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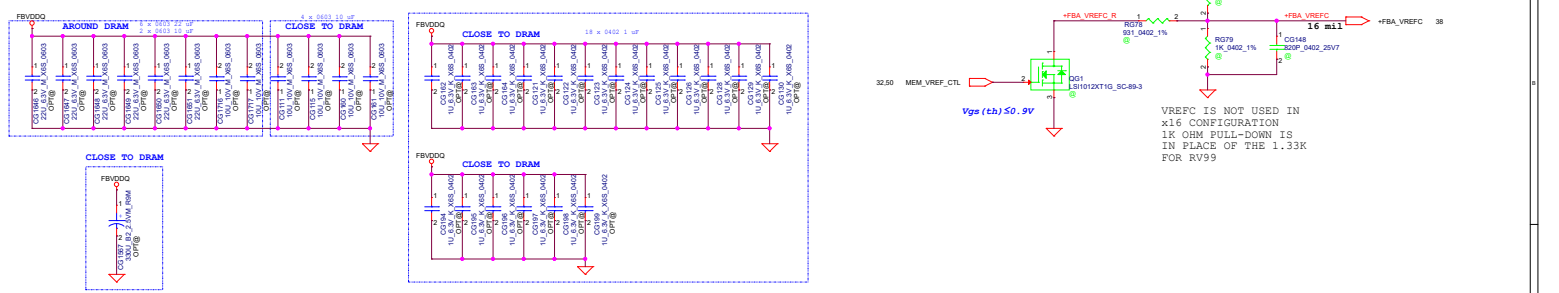
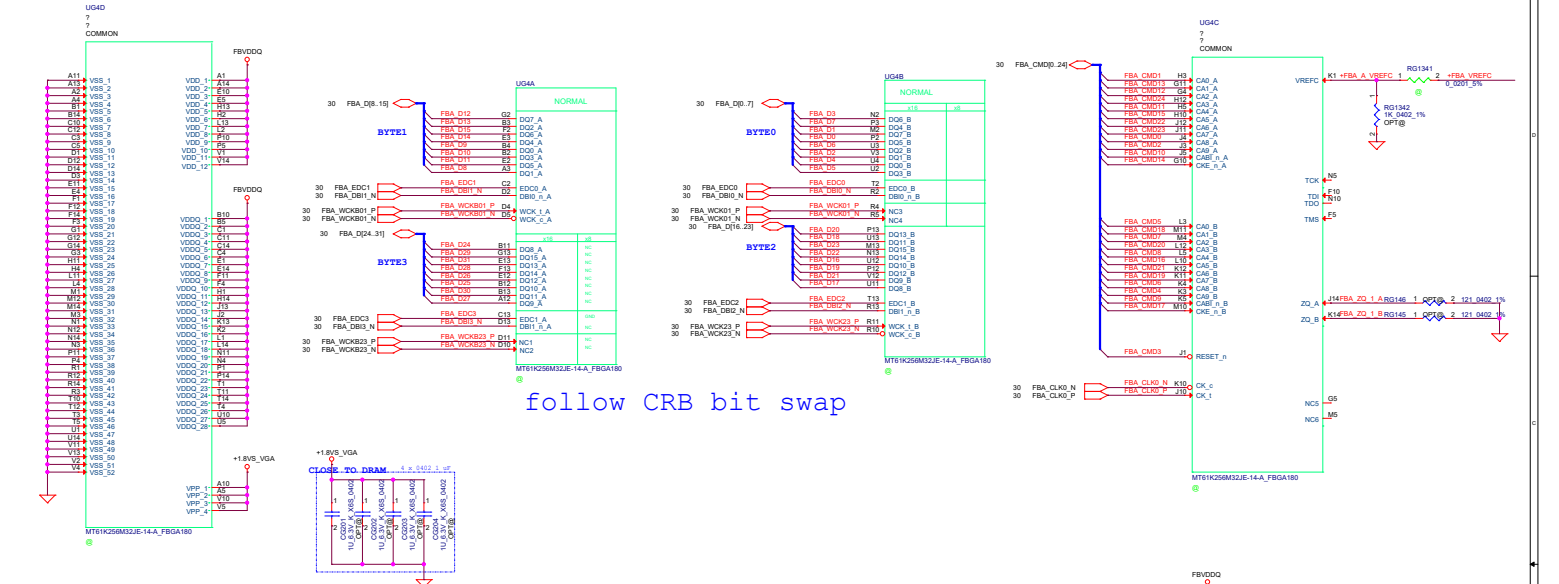




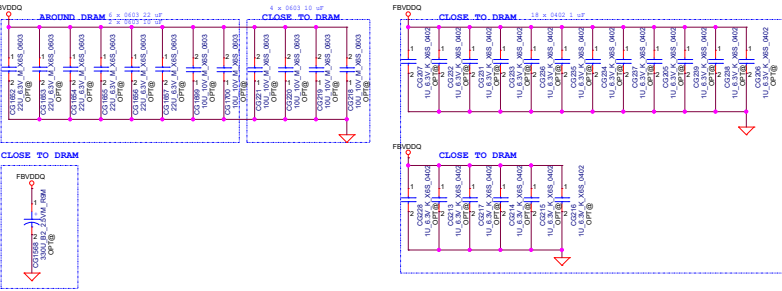
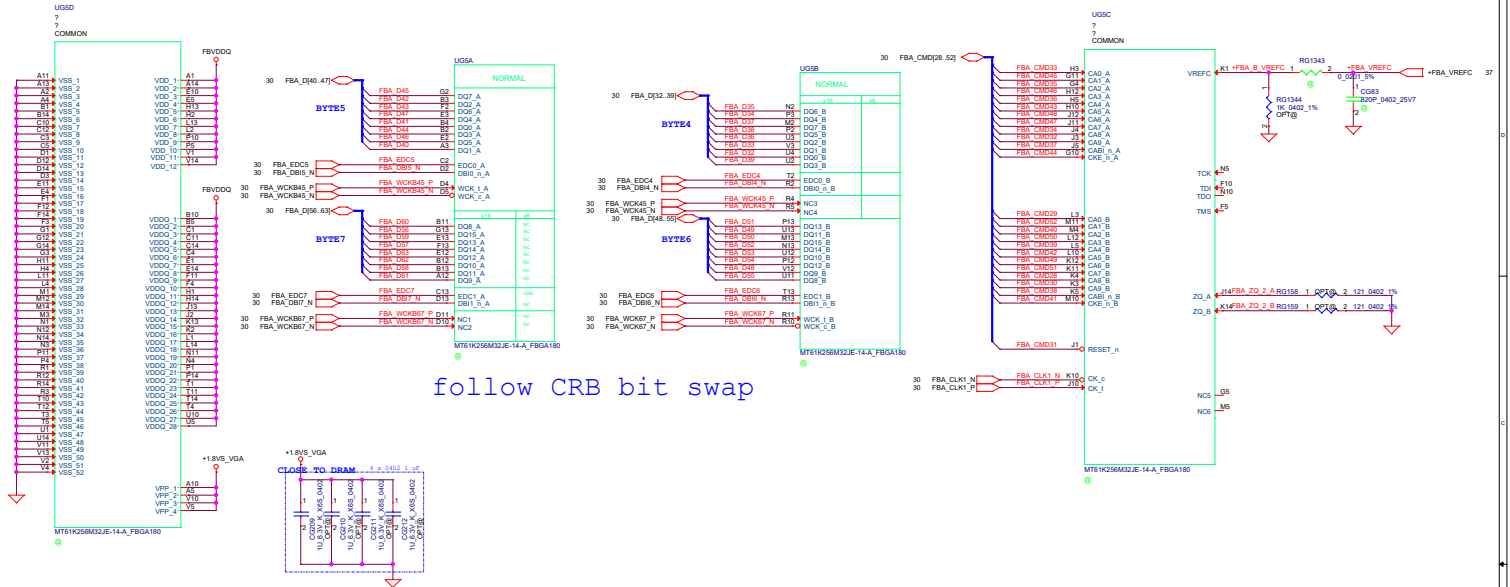


Security Classification	LCFC Highly Confidential Information		Rev
Revised Date	20180402	Original Date	20180402
Title			AVAS-G1_POWER_V000
Part Number			7550
Rev			1.1



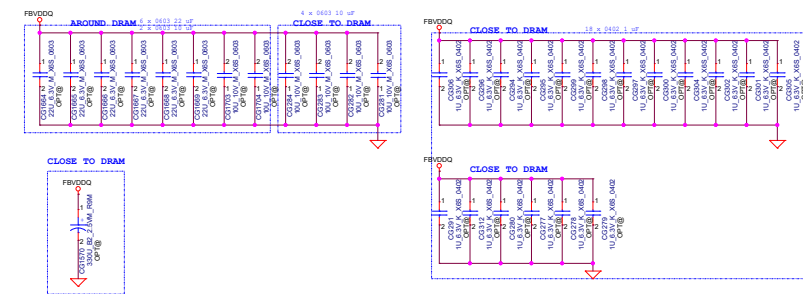
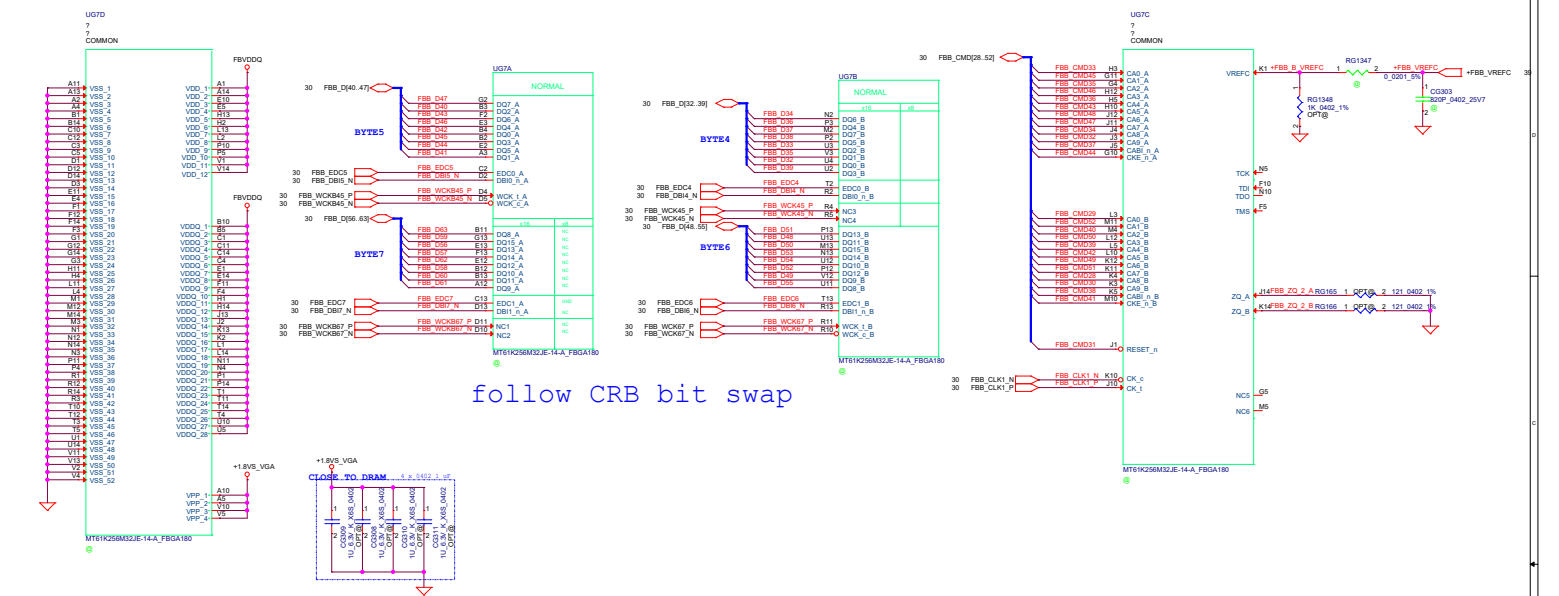


Security Classification				Title	
LCFC Highly Confidential Information				M18E-G1_GDOR6_A_31_01	
Issued Date	2018/08/02	Deciphered Date	2018/08/02	Document Number	Y550
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				Date	Monday, March 24, 2021
				Sheet	37 of 110

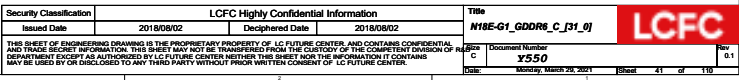


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				Size C		Document Number		Rev	
				Y550				0.1	
				Date		Monday, March 24, 2021		Sheet 35 of 110	

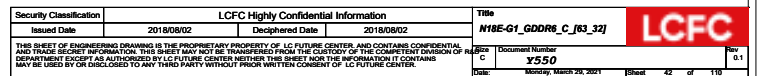


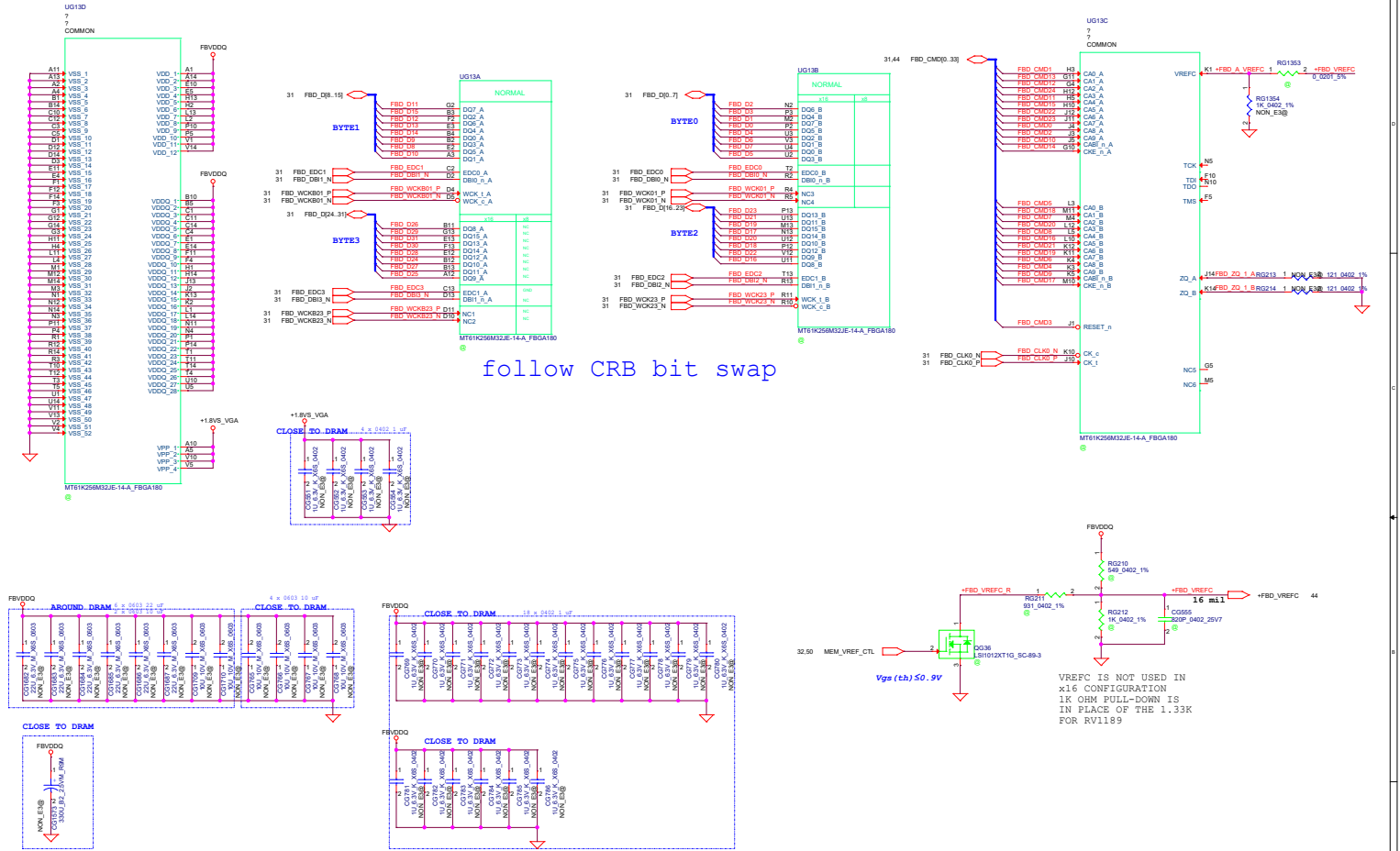


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				Scale	Monday, March 24, 2021
				Sheet	45 of 110

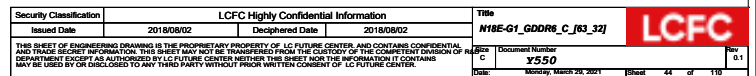


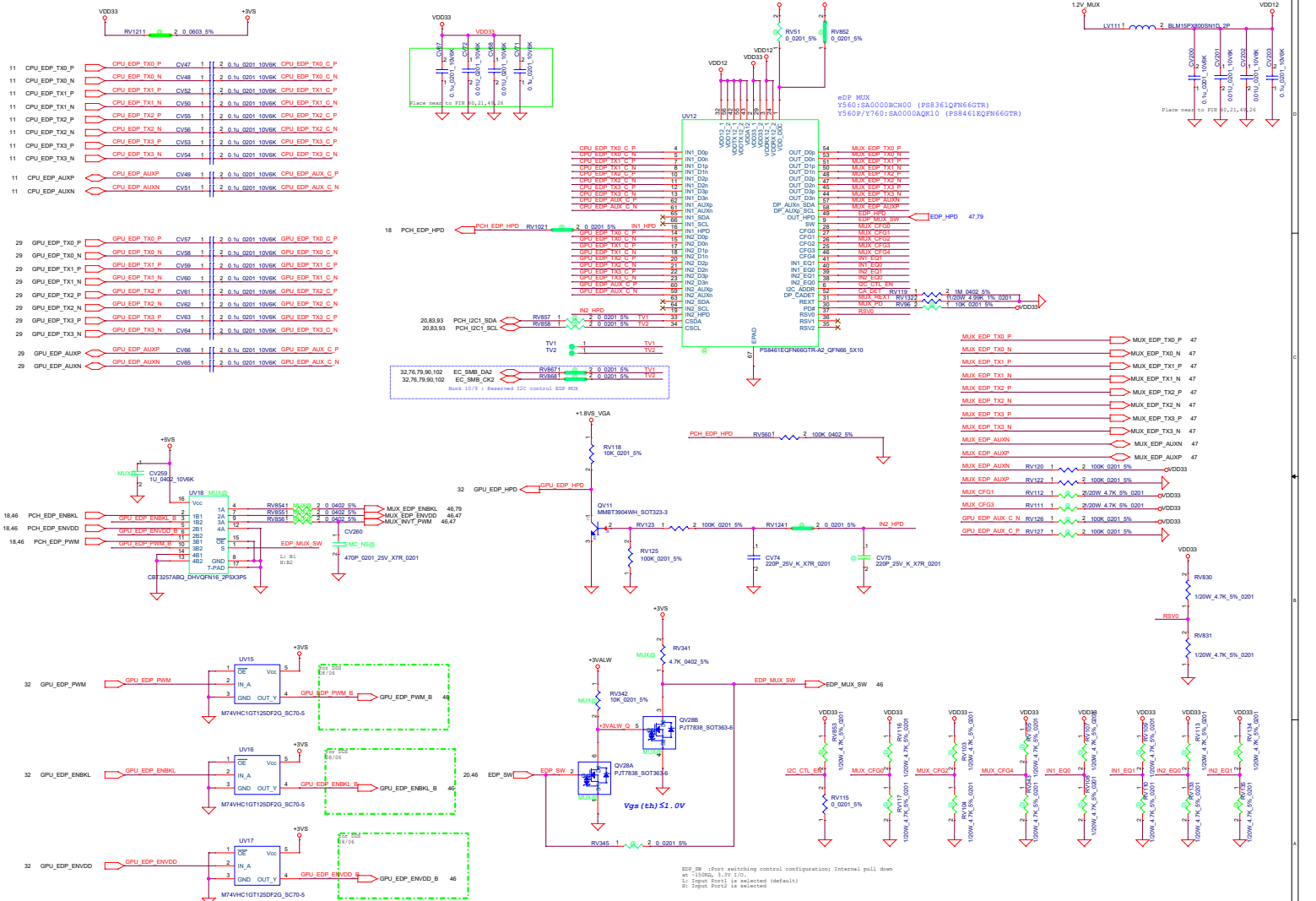






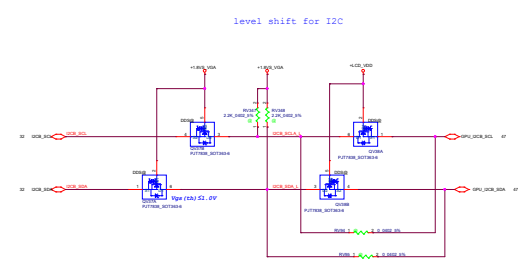
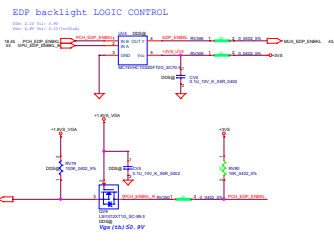
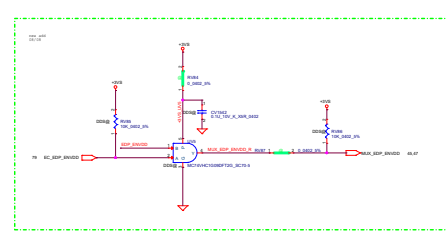
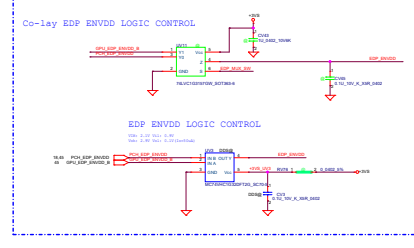
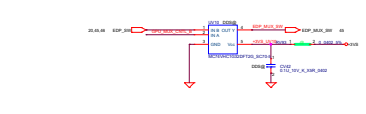
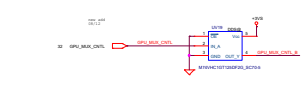
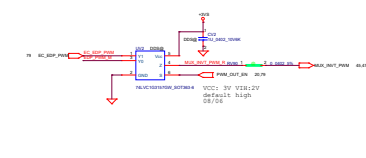
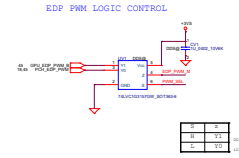
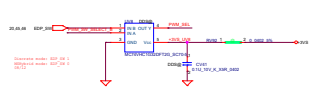
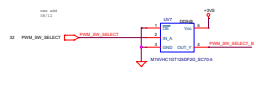
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				Rev		Rev	
				0.1		0.1	
				Date		Monday, March 24, 2021	
				Sheet		43 of 110	





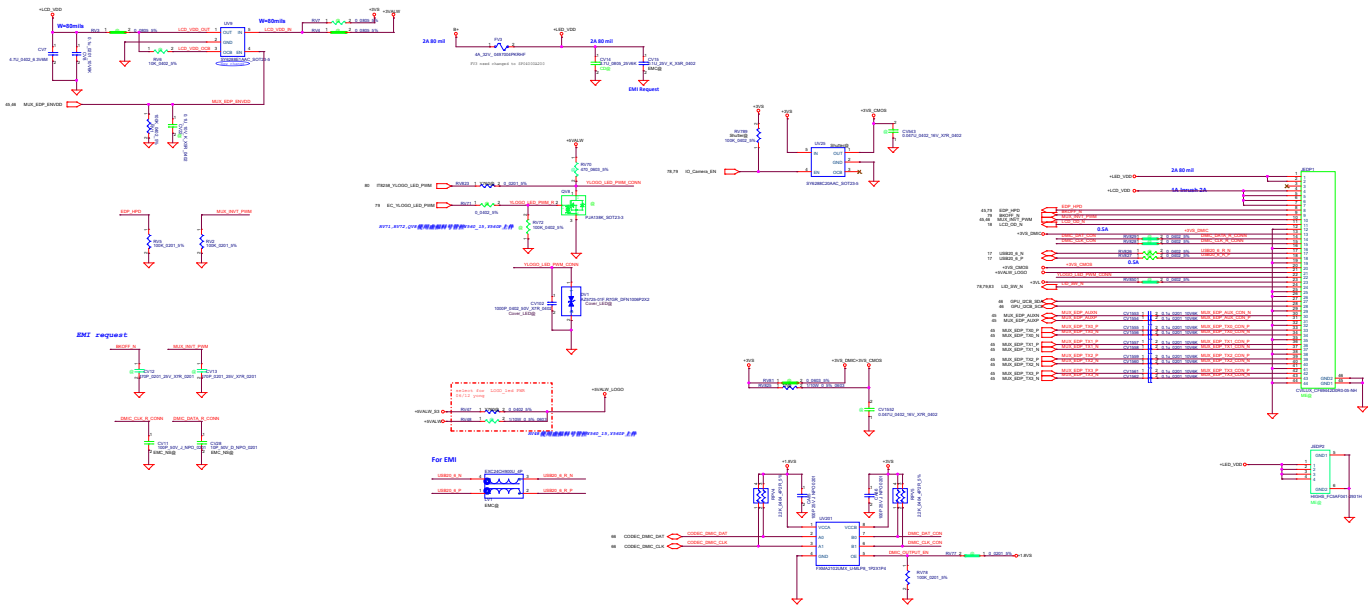
EDP\_SW (Port switching control configuration): Internal pull down  
W: 1000W, 0.001%  
L: Input Port is selected (default)  
B: Input Port is selected

Security Classification			LCFC Highly Confidential Information		Title	
Issued Date			2019/07/02		Deciphered Date	
					2020/02/24	
					EDP MUX	
					Document Number	
					Y540	
					Rev	
					1.0	
					Date	
					Monday, March 24, 2021	
					Sheet	
					45 of 116	



Security Classification	LC Future Center Secret Data	Rev
Secret	20180802	01
Design Date	Design Date	Design Date
20180802	20180802	20180802
DC V TO VS INTERFACE		
25.50		

# LCD POWER CIRCUIT



Security Classification	LCFC Highly Confidential Information		Item
Revised Date	20190702	Completed Date	20190804
<small>                     This document contains information that is highly confidential and proprietary to LCFC. It is intended for internal use only. It is not to be distributed outside of LCFC. It is not to be used for any other purpose. It is not to be reproduced or transmitted in any form or by any means, electronic, mechanical, photocopying, recording, or by any information storage and retrieval system, without prior written permission from LCFC.                 </small>			ADP CMOS Touch screen
			LCFC
			23-60
			1.1

Security Classification		LC Future Carrier Secret Data		Title	
Secret Date		20180402		Designated Date	
20180402		20180402		ADDP CMOS/Touch screen	
ADDP		2350		2350	

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Title
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**<Title>**

Size

**A**

Document Number

<Doc>

Rev

<RevCo

Date:

Monday, March 29, 2021

Sheet

49

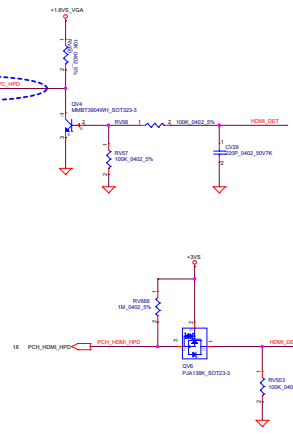
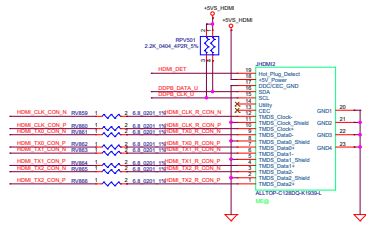
of

110



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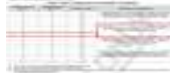
del NVS12,NVS14,NVS16,NVS17,NVS19,NVS20,NVS22,NVS23,NVS01,NVS02,NVS03,NVS04 ---arthur.chen 12/20



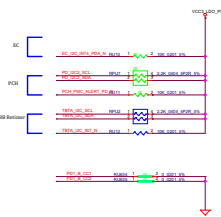
The schematic diagram illustrates the AUX input section of the P47155T56. It features two input channels, AUX1 and AUX2, each with a 1.8V\_GS input, a 10k resistor (RV42, RV40), a 0.047uF capacitor (C42, C40), and a 10k resistor (RV44, RV46). The inputs are connected to the P47155T56 pins 5 (AUX1) and 3 (AUX2). The outputs are connected to the P47155T56 pins 6 (AUX1) and 4 (AUX2). The outputs are labeled AUX1\_DAT and AUX1\_CLK for the left channel, and AUX2\_DAT and AUX2\_CLK for the right channel. The schematic is labeled 'AUX' and 'BT suggestion'.

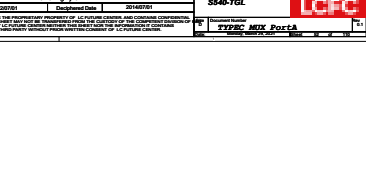
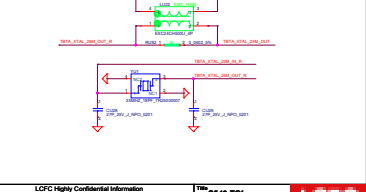
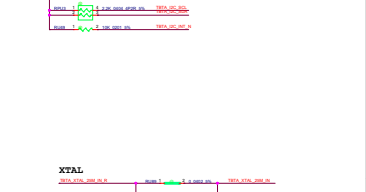
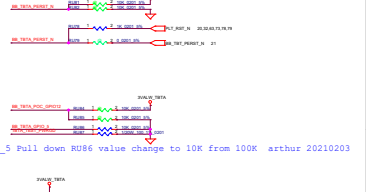
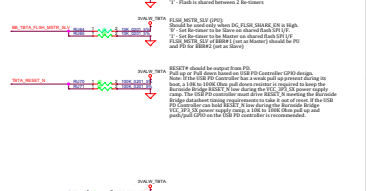
Security Classification	LCFC Highly Confidential Information	Title	HDMI_CONN	LCFC
Issued Date	2019/07/02	Declassified Date	2020/02/24	
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Doc. Name	HDMI_CONN.dwg	Doc. Name	HDMI_CONN.dwg	1.0

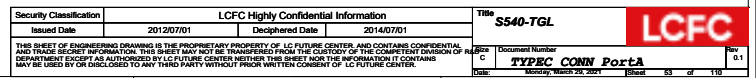
I2C1	Master: AC	TWTR PORT	Dx23
	Slave: PD	TWTC PORT	Dx27
I2C2	Master: PNC	TWTR PORT	Dx23
	Slave: PD	TWTC PORT	Dx27
I2C3	Master: PD	TWTR PORT	I.W.D.
	Slave: RT	TWTC PORT	I.W.D.

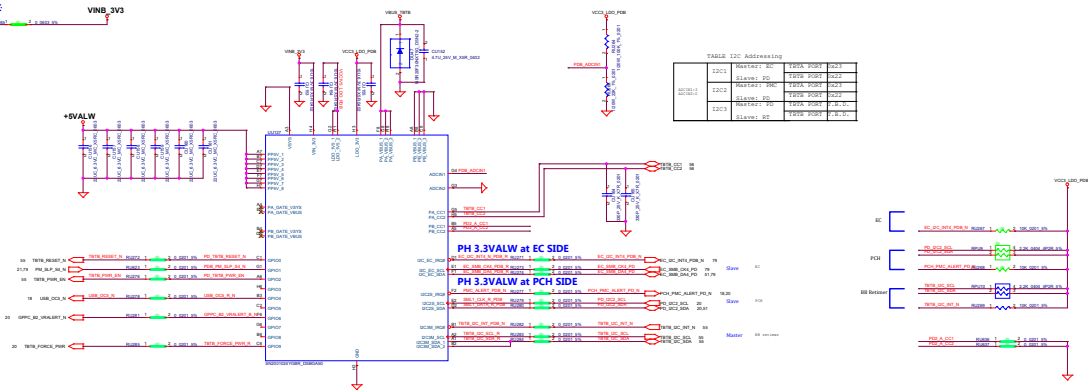


need verify address

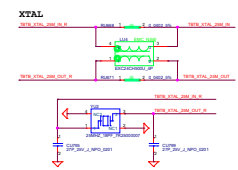
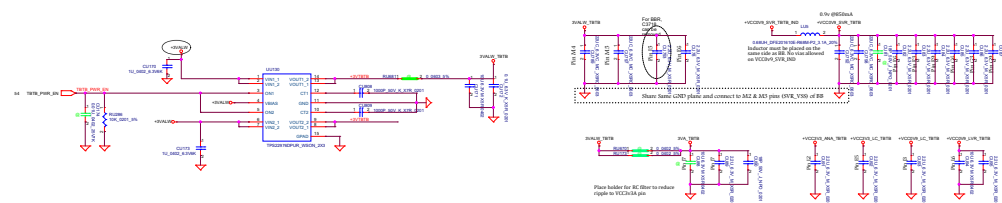
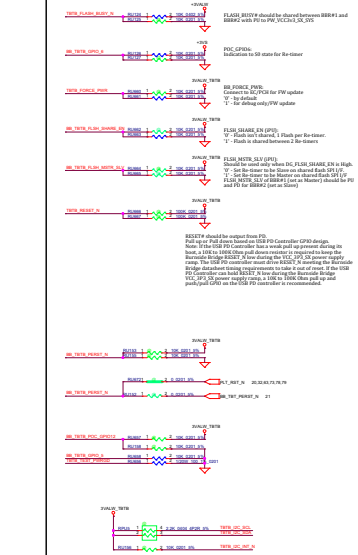
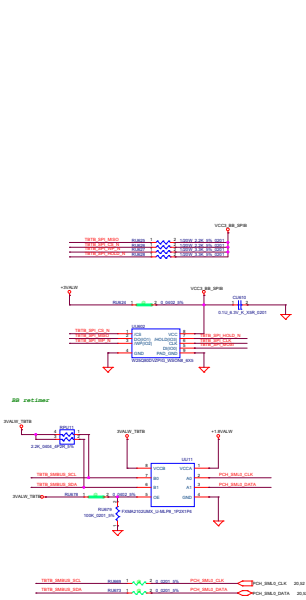


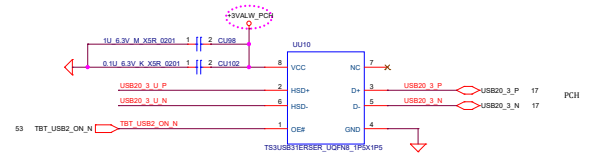
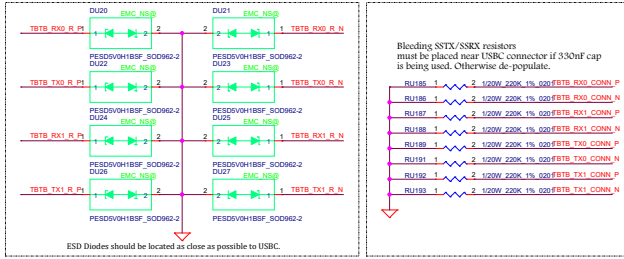
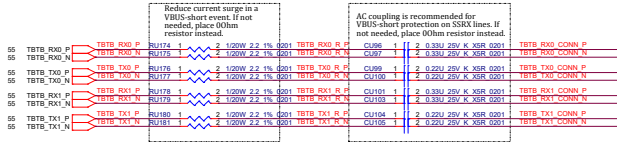




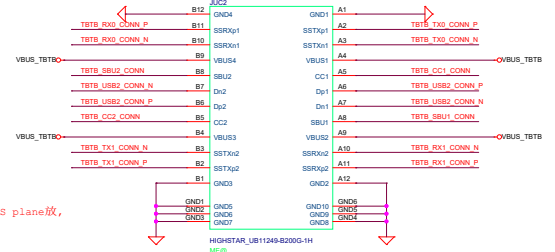
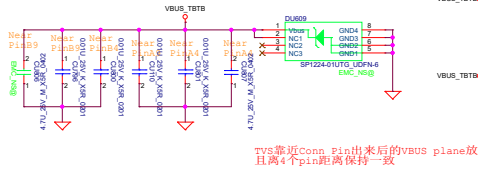
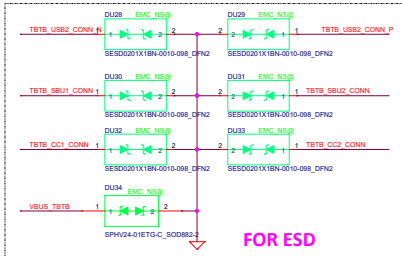
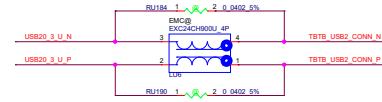


ADDRESS ADDRESS	12C1	Master: MC	DATA PORT	12C3
		Slave: SD	DATA PORT	12C2
	12C2	Master: MC	DATA PORT	12C3
		Slave: SD	DATA PORT	12C2
	12C3	Master: MC	DATA PORT	12C2
		Slave: SD	DATA PORT	12C1

[illegible][illegible]

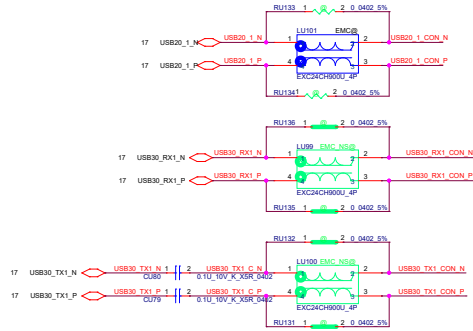
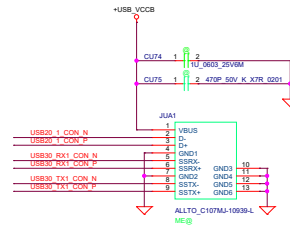
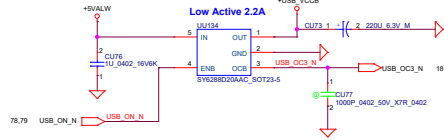


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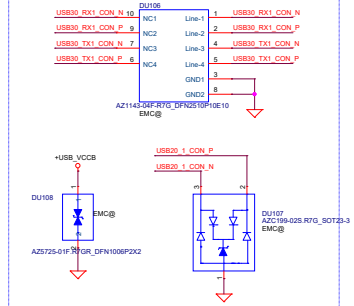


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Issued Date		2012/07/01		Deciphered Date		2014/07/01		Document Number		Rev	
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# USB3.1 PORT x2

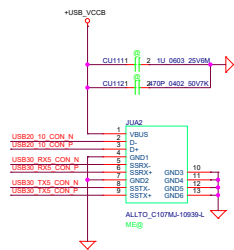


## EMC close to USB Conn

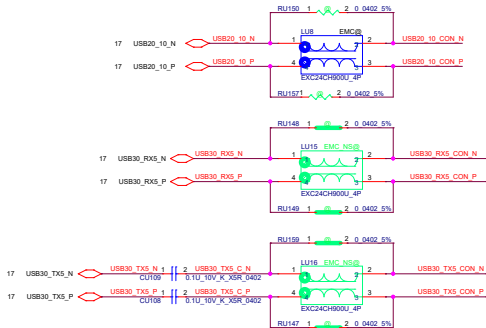
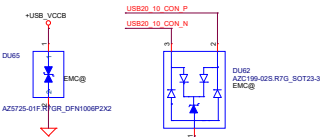
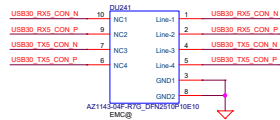


Security Classification		LC Future Center Secret Data		Title	
Issued Date	2018/08/02	Deciphered Date	2018/08/02	USB2.0	
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				Date	Monday, March 24, 2021
				Sheet	87 of 110
				Rev	0.1

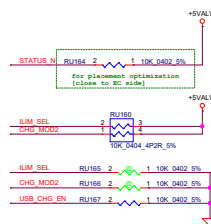
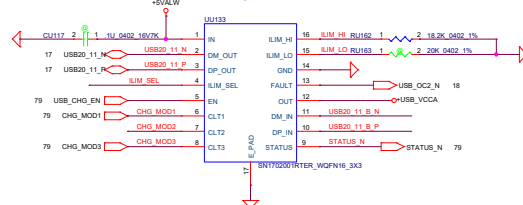
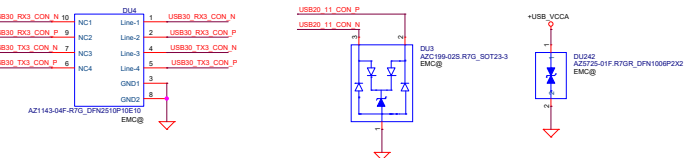




### EMC close to USB Conn



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Issued Date		Deciphered Date		USB2.0	
2018/08/02		2018/08/02		Document Number	
C		Y550		Rev	
Date		Monday, March 24, 2021		Sheet 88 of 110	



CLT1	CLT2	CLT3	ILUM_SEL	MOD	
0	0	0	X	DCR	OUT held low
1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2	Data Connected
1	1	0	X	SDP1	Data Connected
0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Boot	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 charging Mode
0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active

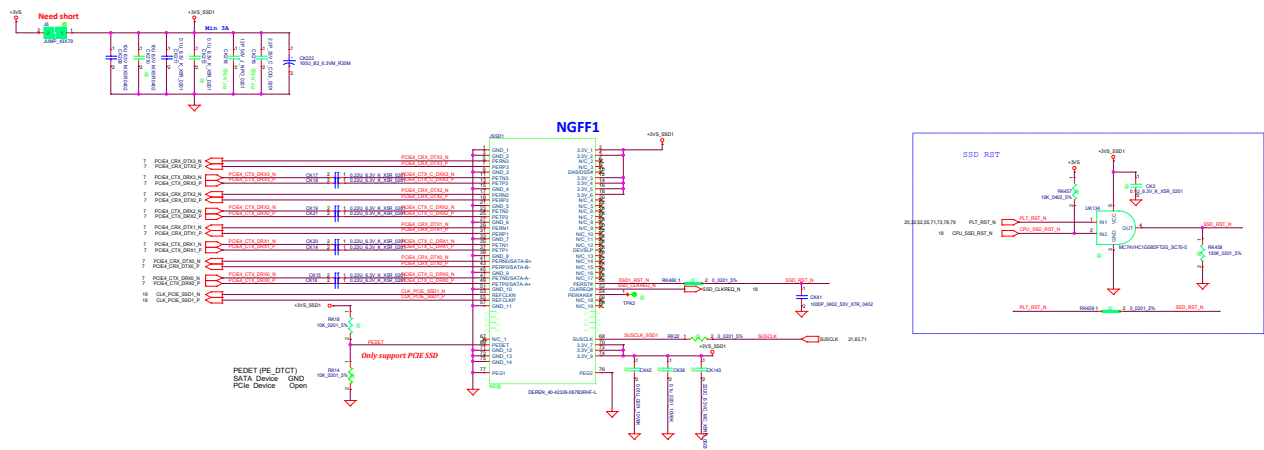
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Issued Date		Deciphered Date		2018/08/02	
2018/08/02		2018/08/02		USB2.0/USB3.0 PORT (LEFT)	
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				Y550	1



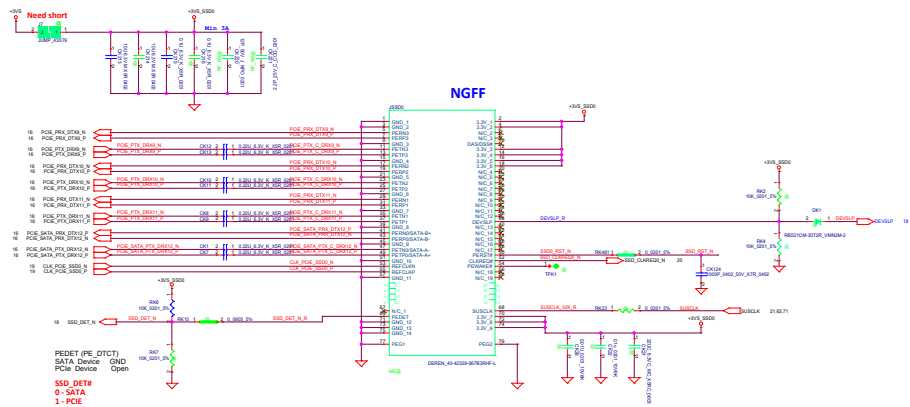
A	B	C	D	E	F	G	H


A	B	C	D	E	F	G	H

### *M.2 SSD(PCIE GEN4 from CPU)*



### ***M.2 SSD(SATA/PCIE Gen3 from PCH)***



Security Classification	LC Future Center Secret Data		Title	NGFF WLAN	
Issued Date	2018/08/02	Declassified Date	2018/08/02		
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Approved Date: 2018/08/02				Page 1 of 1	

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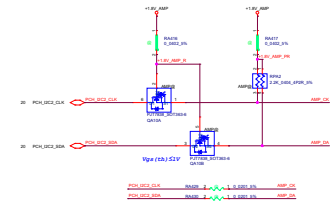
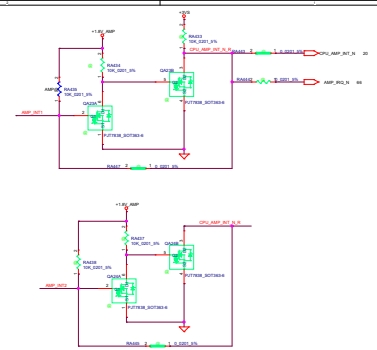
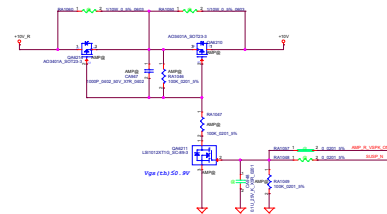
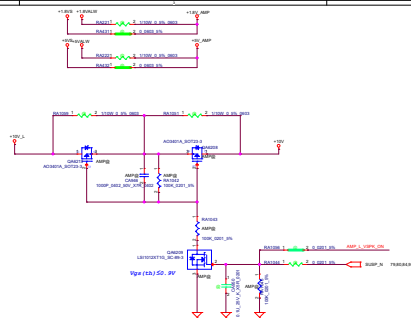
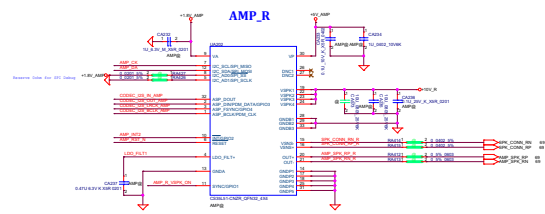
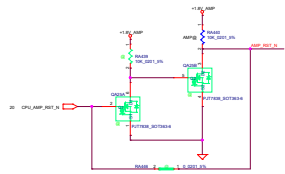
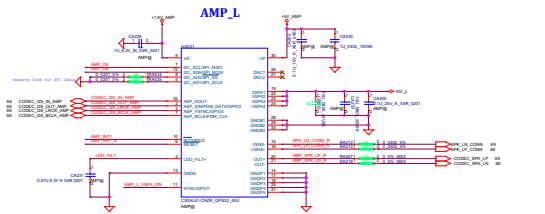
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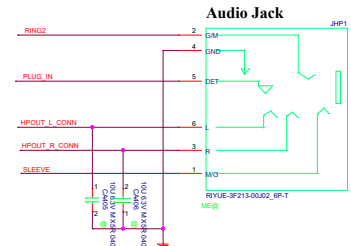
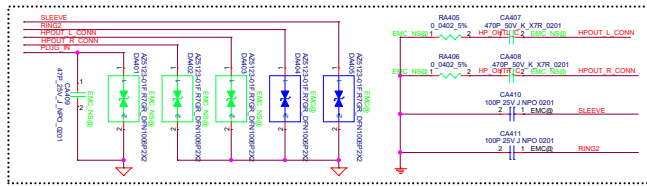
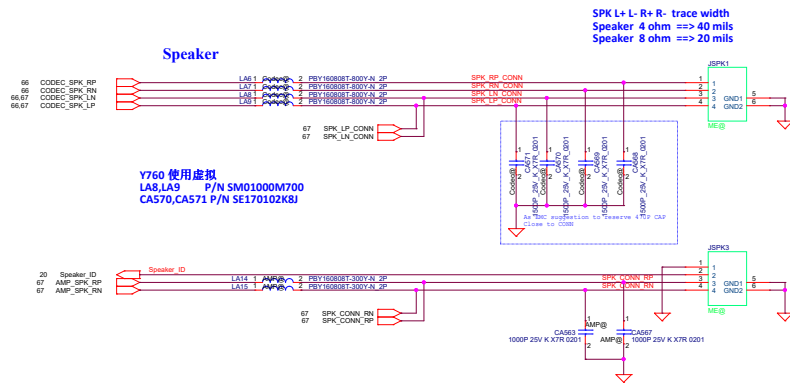
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<small>Monday, March 29, 2021</small>				





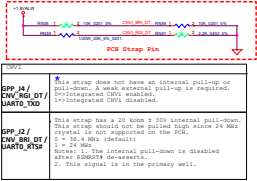


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				Audio DSP	0.2	
			Date	Monday, March 24, 2021	Sheet 88 of 110	




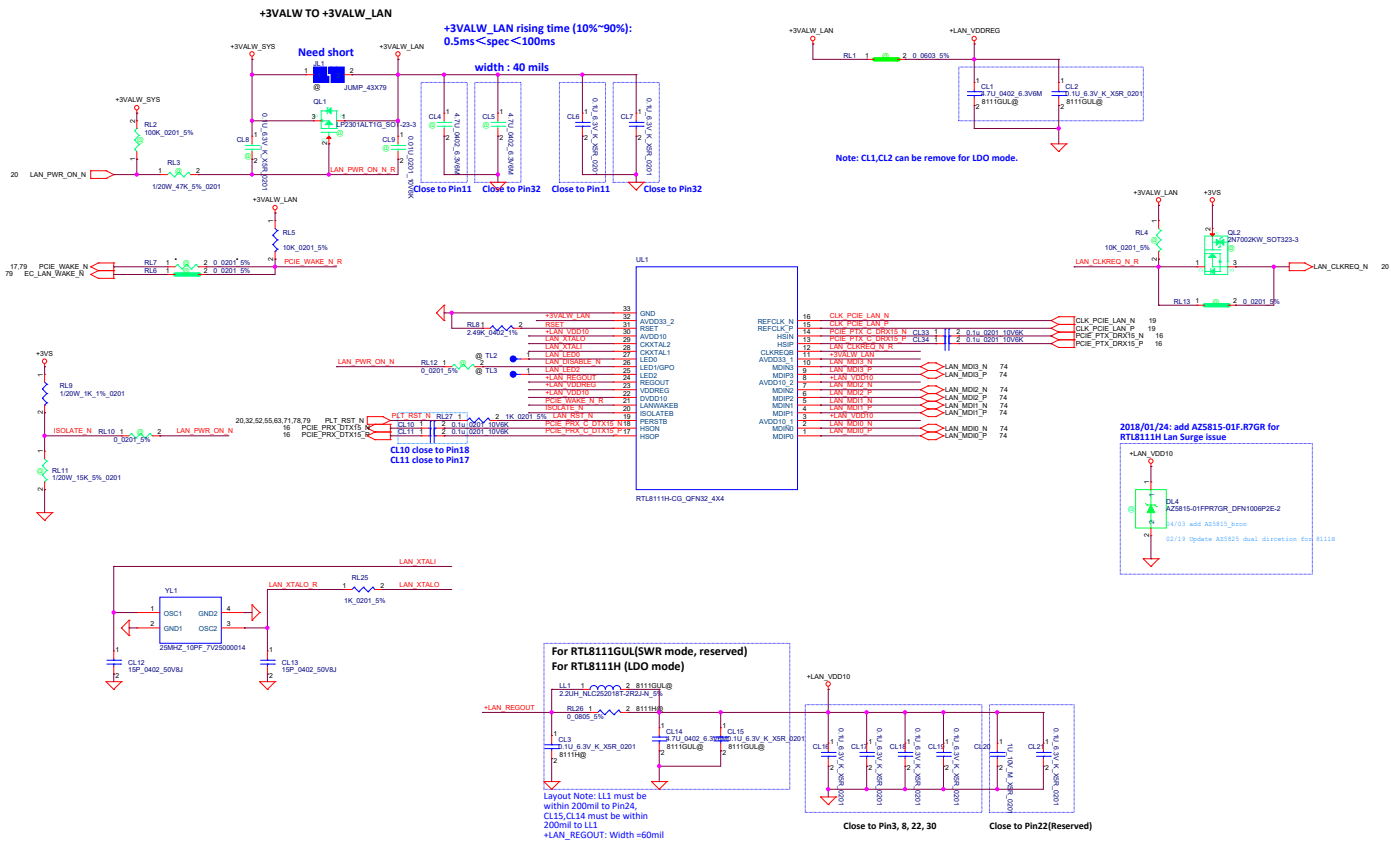
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Date: Monday, March 24, 2021					Sheet 89 of 110

### Mini-Express Card(WLAN/WiMAX)

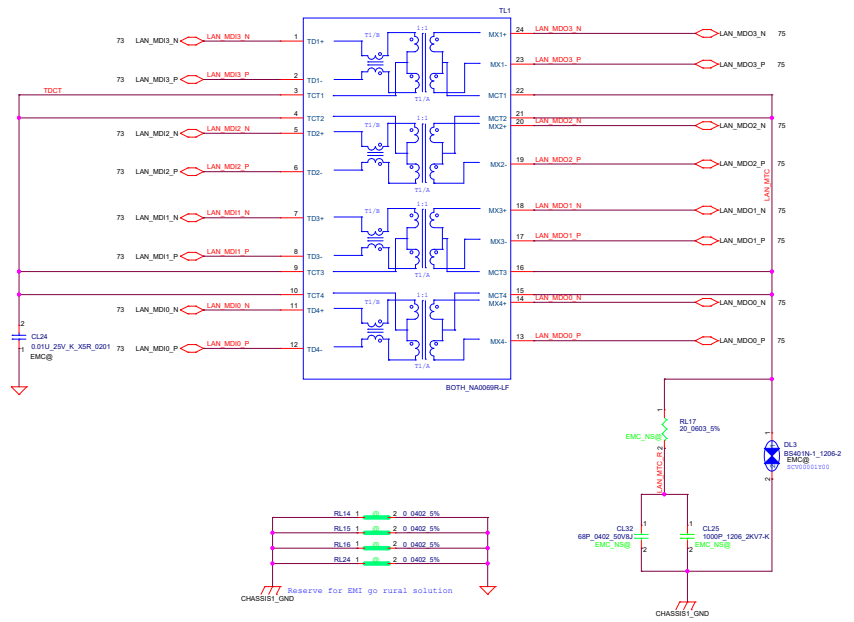
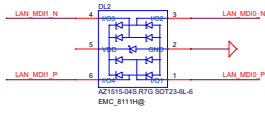
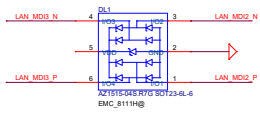


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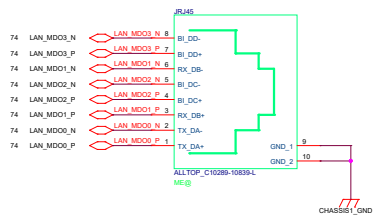
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Size		Document Number		Rev		0.2
Date:		Monday, March 26, 2021		Sheet		72 of 110



DL1/DL2  
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Place Close to TL1



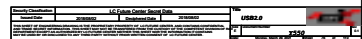
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				Y540	1.0
				Date	Monday, March 24, 2021
				Sheet	74 of 110

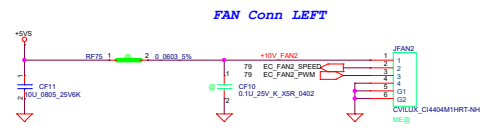


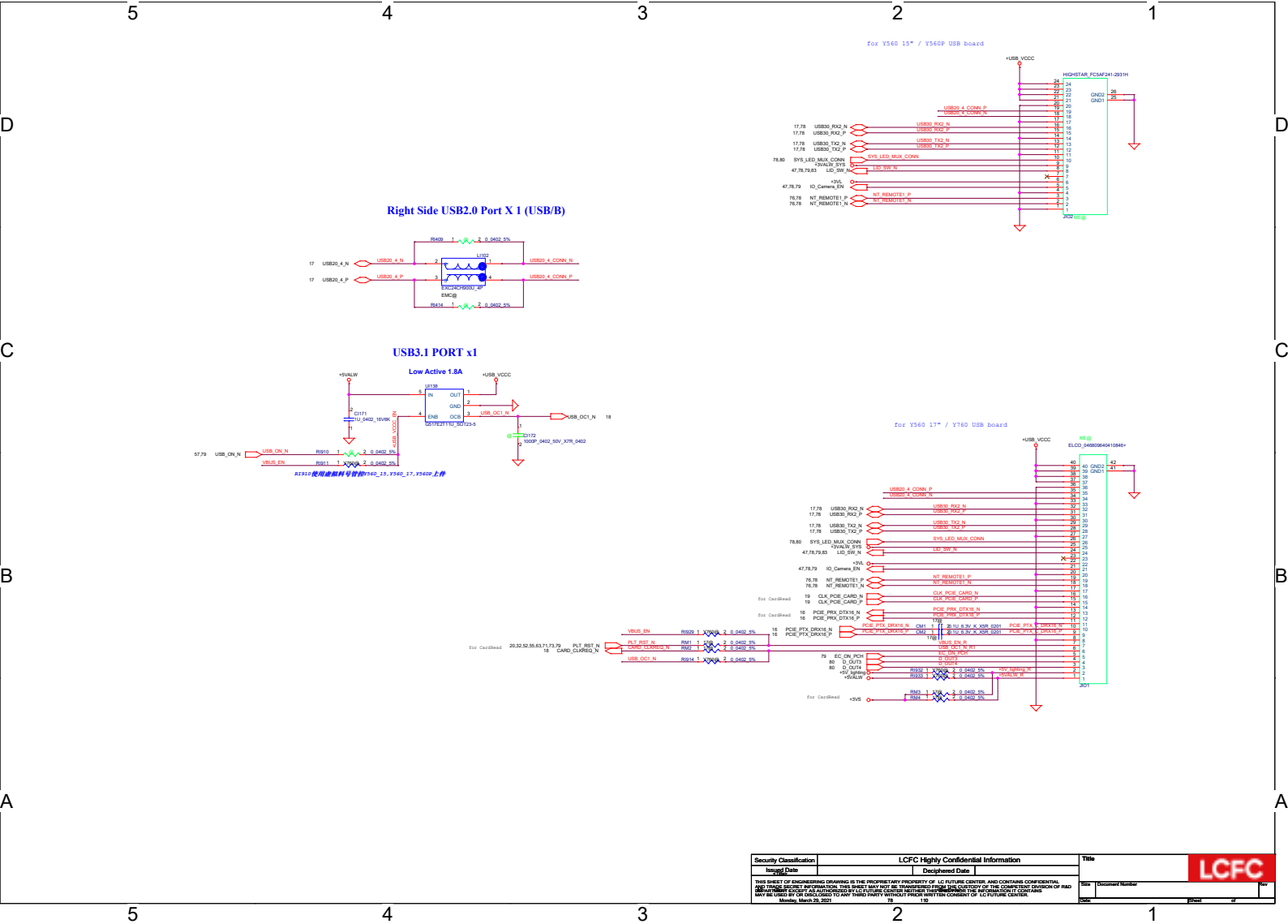
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					Y540	1.0
				Date	Monday, March 24, 2021	
				Sheet	75	of 110

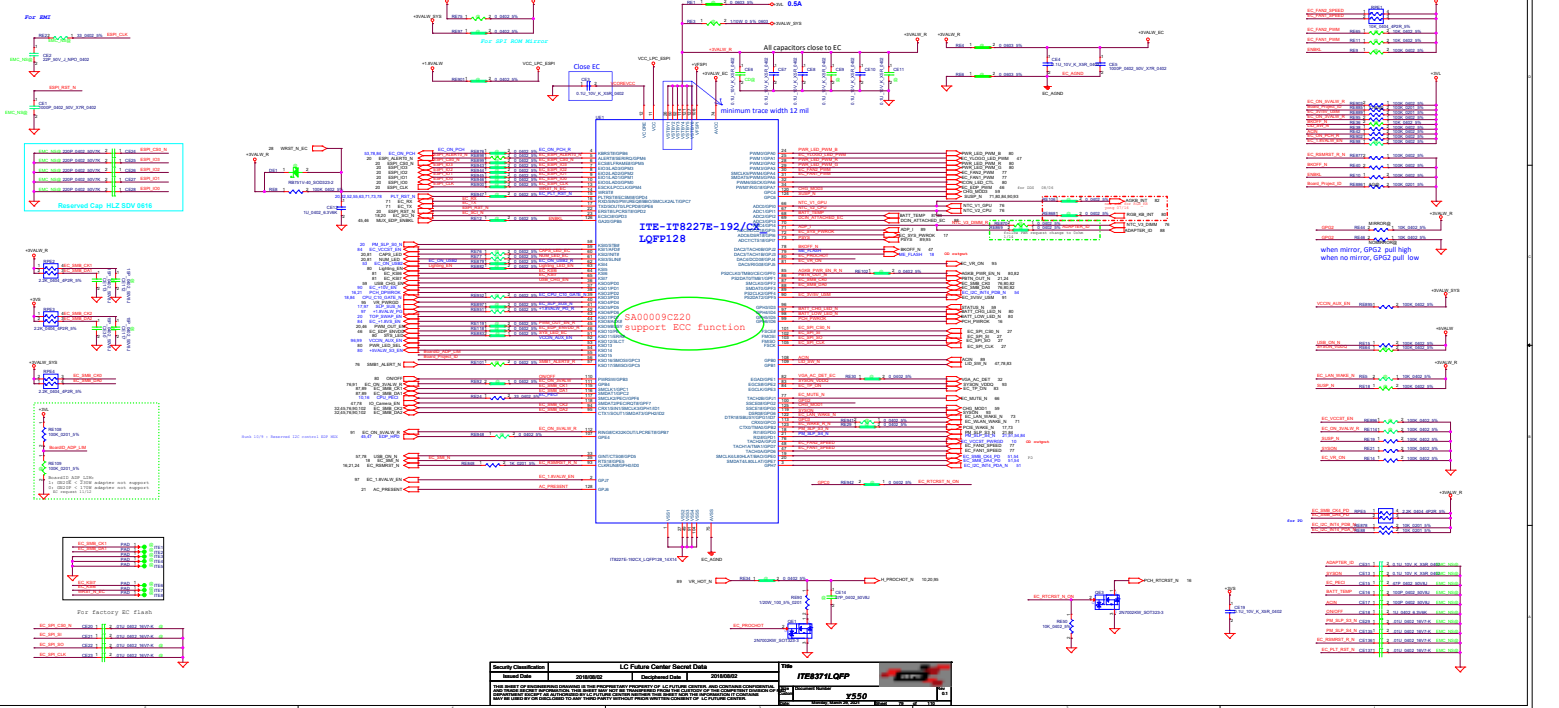


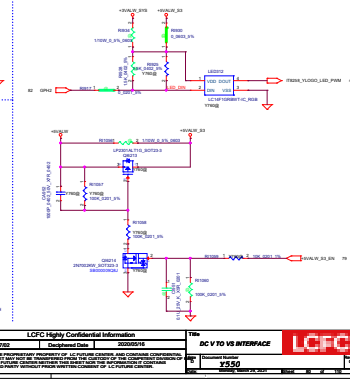
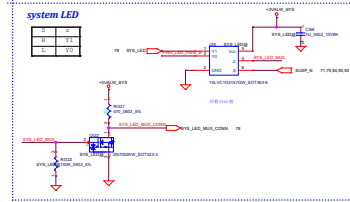
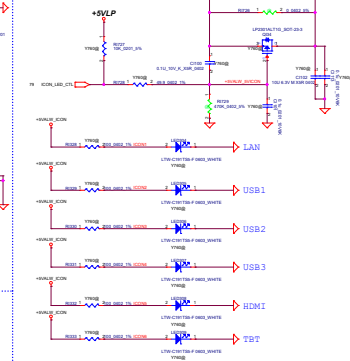
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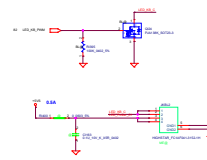




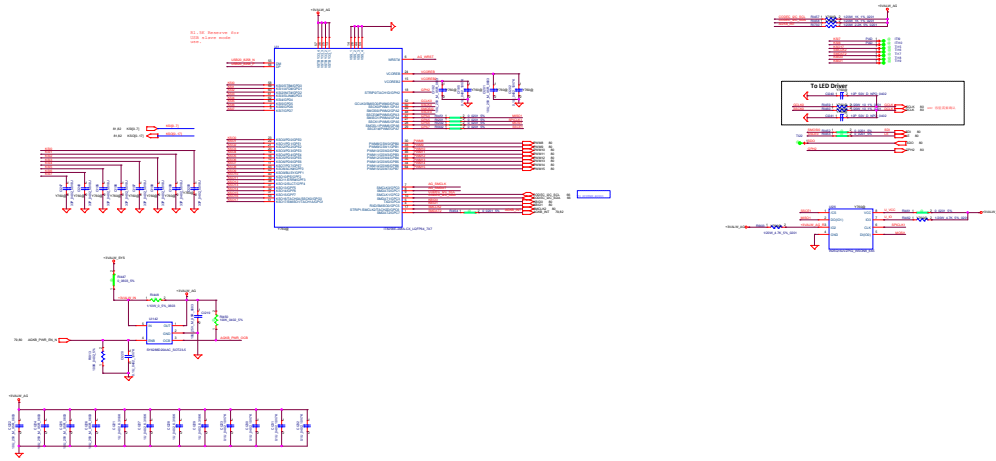


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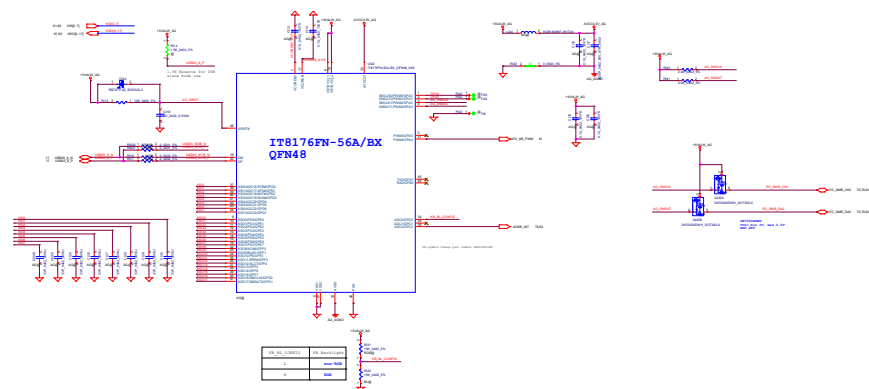
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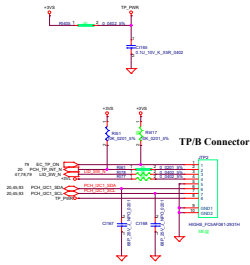
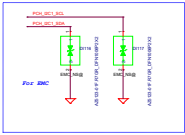


## IT8258

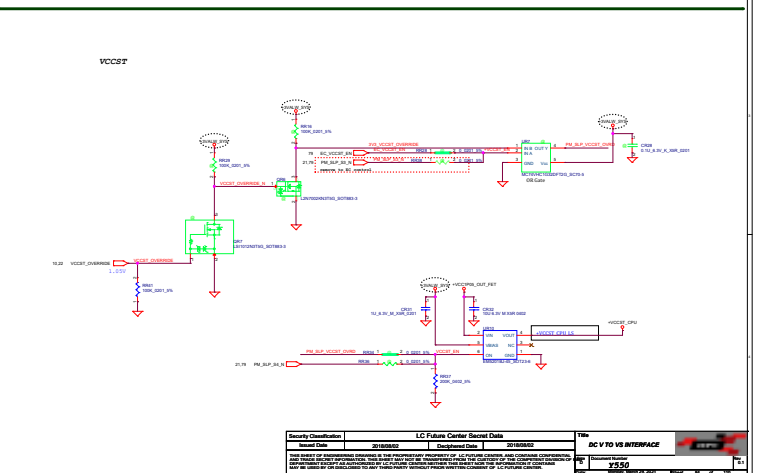
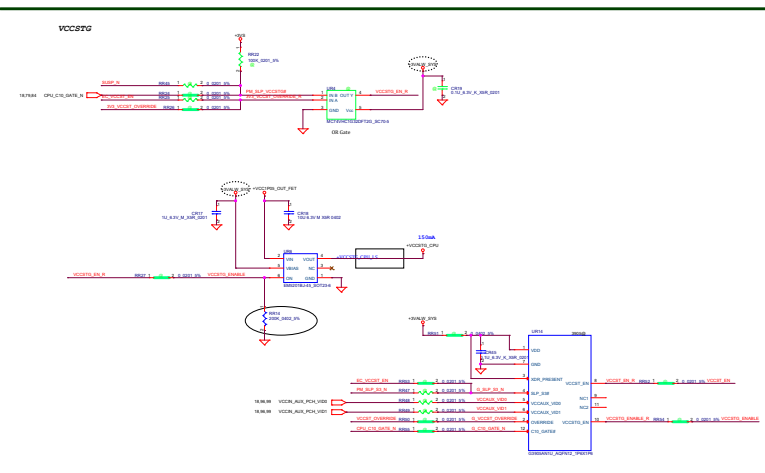
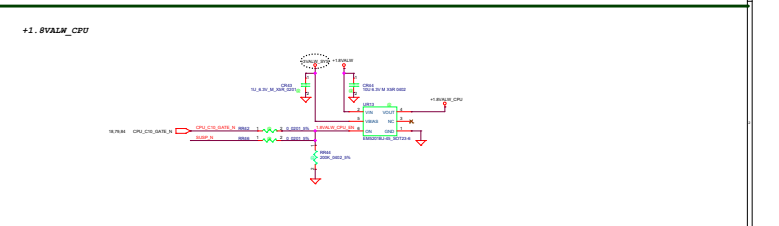
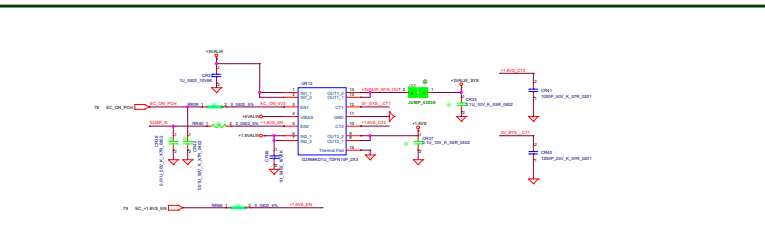
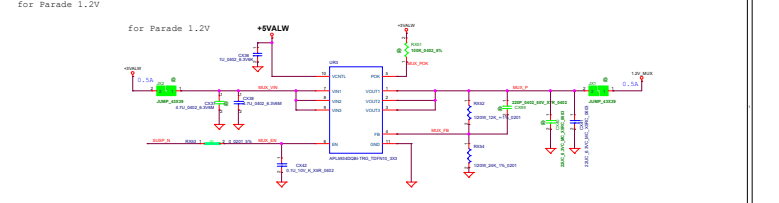
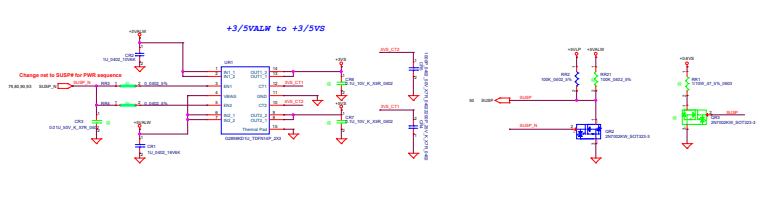


## IT8176






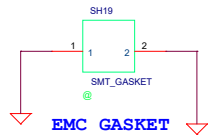
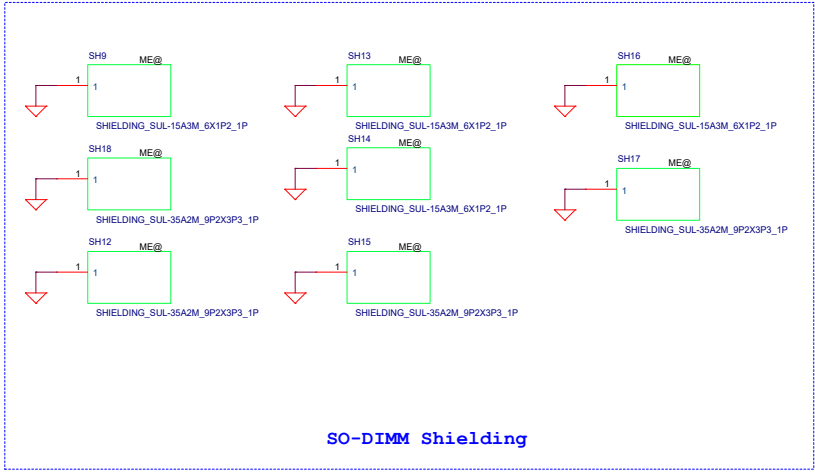
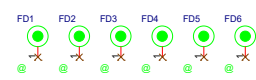
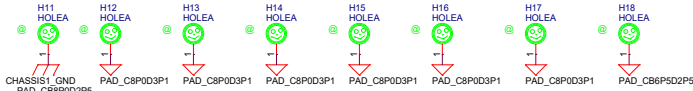
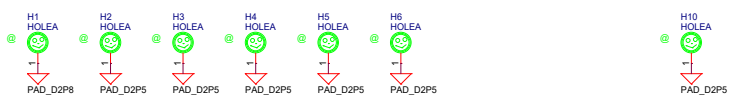




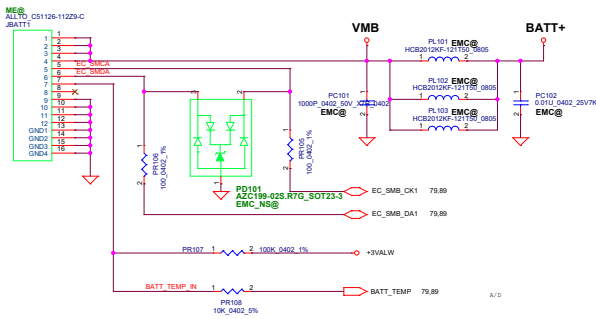


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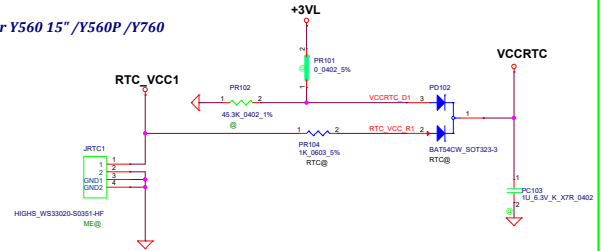
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Security Classification	LC Future Center Secret Data			Title	Yx60 TGL-H																																			
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				Date:	Monday, March 28, 2021	Sheet	85	of 110																																
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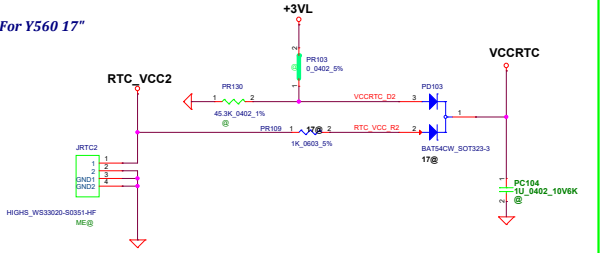
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				Date:	Monday, March 28, 2021	ISheet 88 of 110



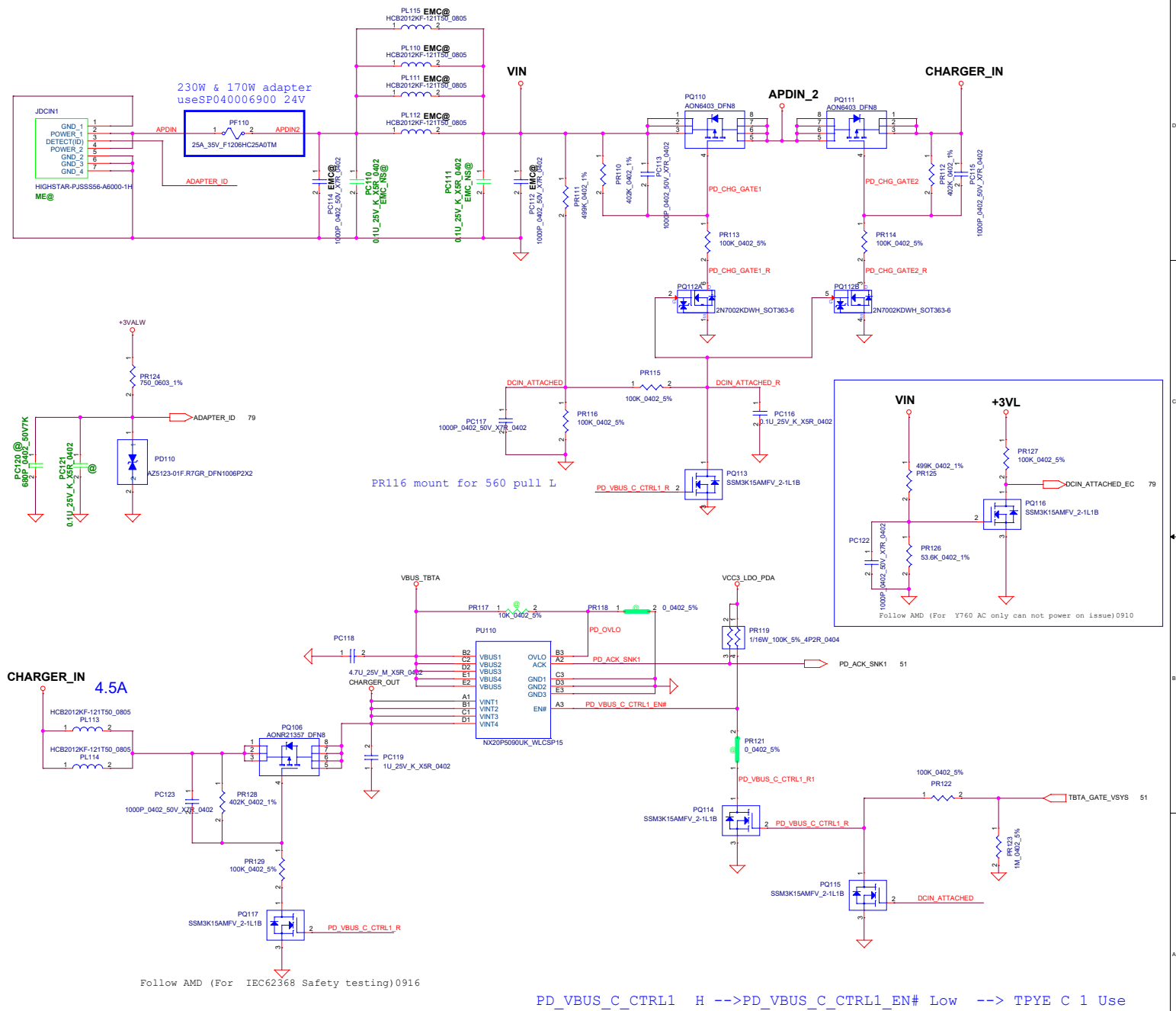
For Y560 15" /Y560P /Y760



For Y560 17"



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PD\_VBUS\_C\_CTRL1 H --> PD\_VBUS\_C\_CTRL1\_EN# Low --> TPYE C 1 Use

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Date	Monday, March 29, 2021	Sheet	88	of	110	

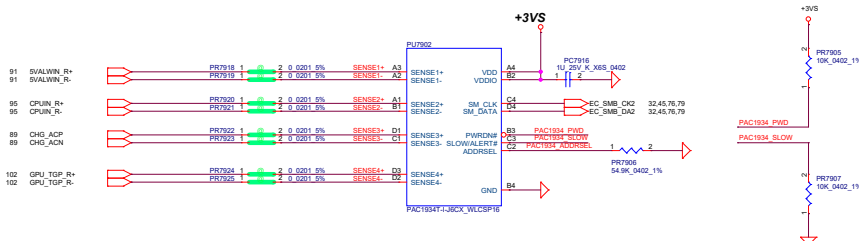
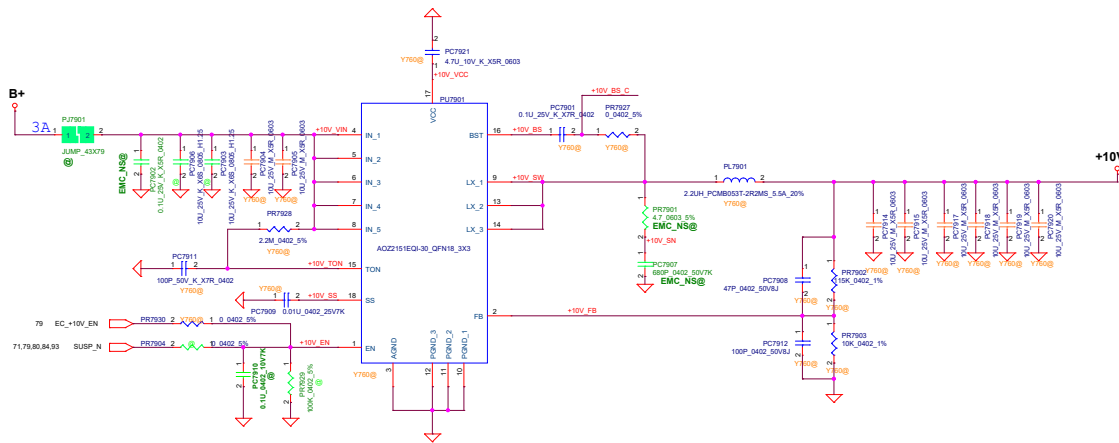
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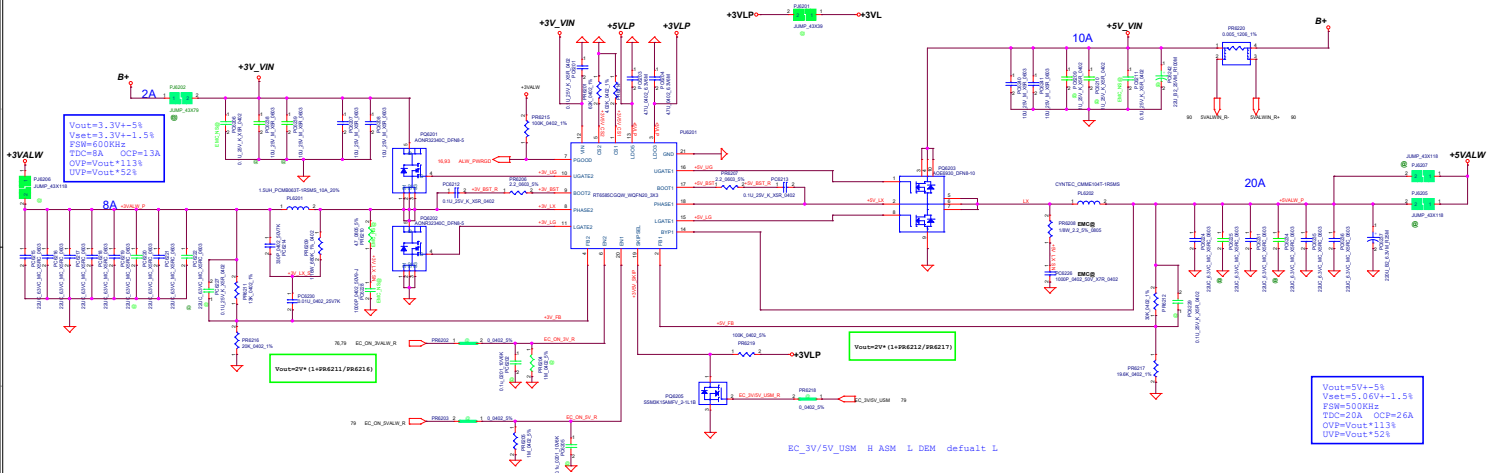
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Security Classification	LC Future Center Secret Data	Title	PWR-charger
Issued Date	2018/09/02	Declassified Date	2018/09/02
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Doc	Document Number	Y550	Rev
Doc	Rev	Rev	Rev



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Size		Document Number		Rev	
Custodian		Y560 AMD		01	
Date		Monday, March 29, 2011		10:58	
Page		80		of 110	



	RT6585C	RT6575D&TPS51275B
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3V FSW	600K	355K
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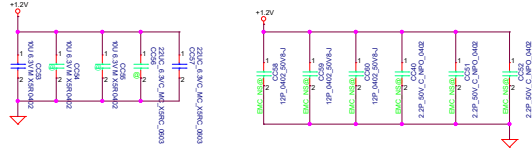


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				Date	Monday, March 24, 2021
				Sheet	92 of 110



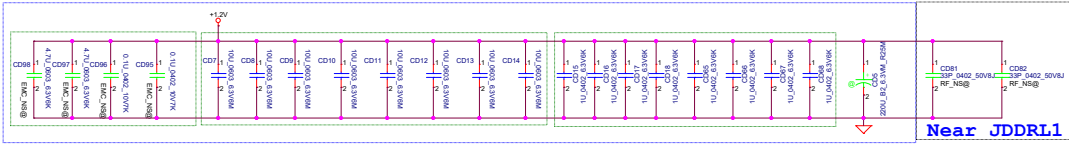


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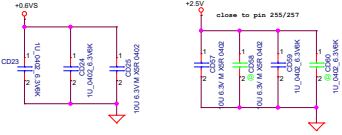
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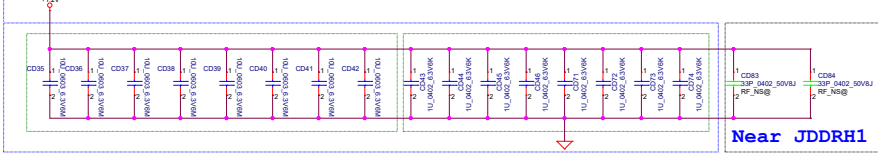
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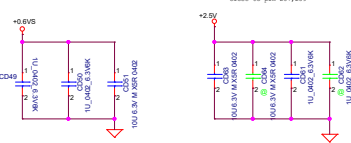
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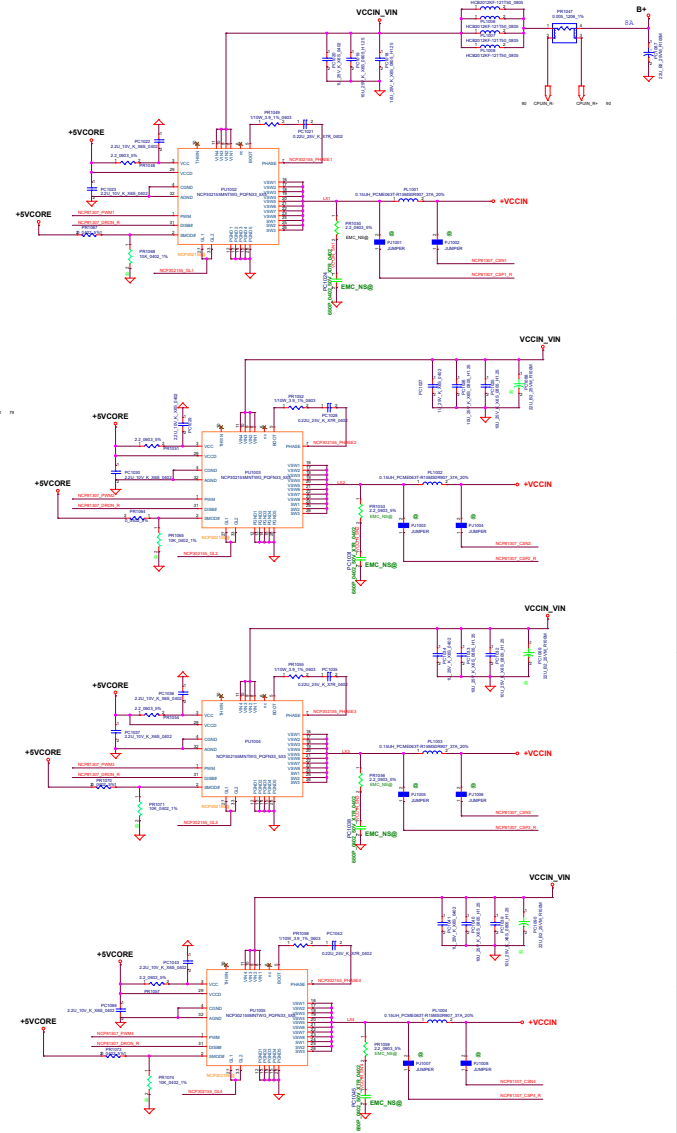
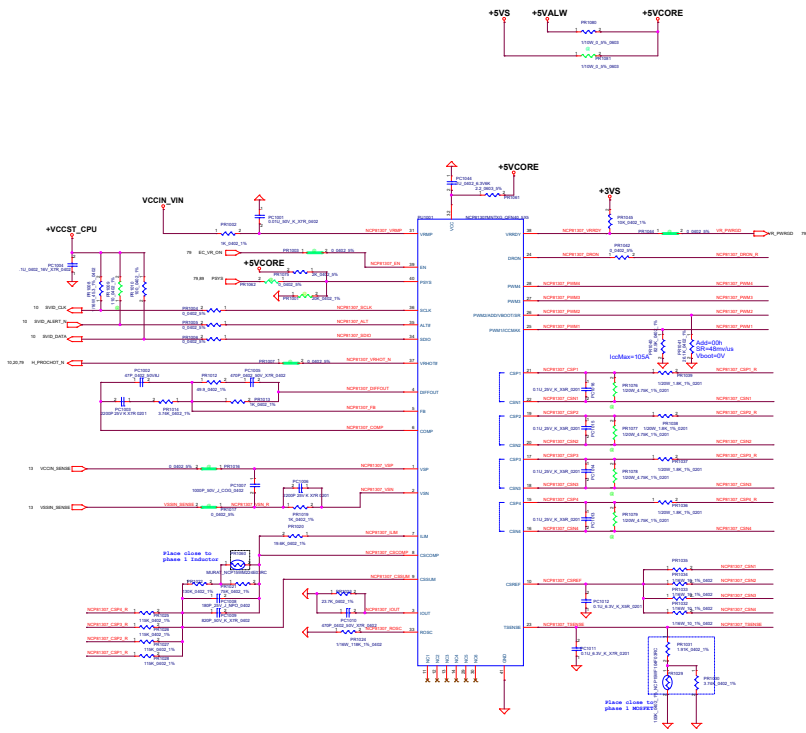


Near JDDR1

Layout Note:  
Place near DIMM

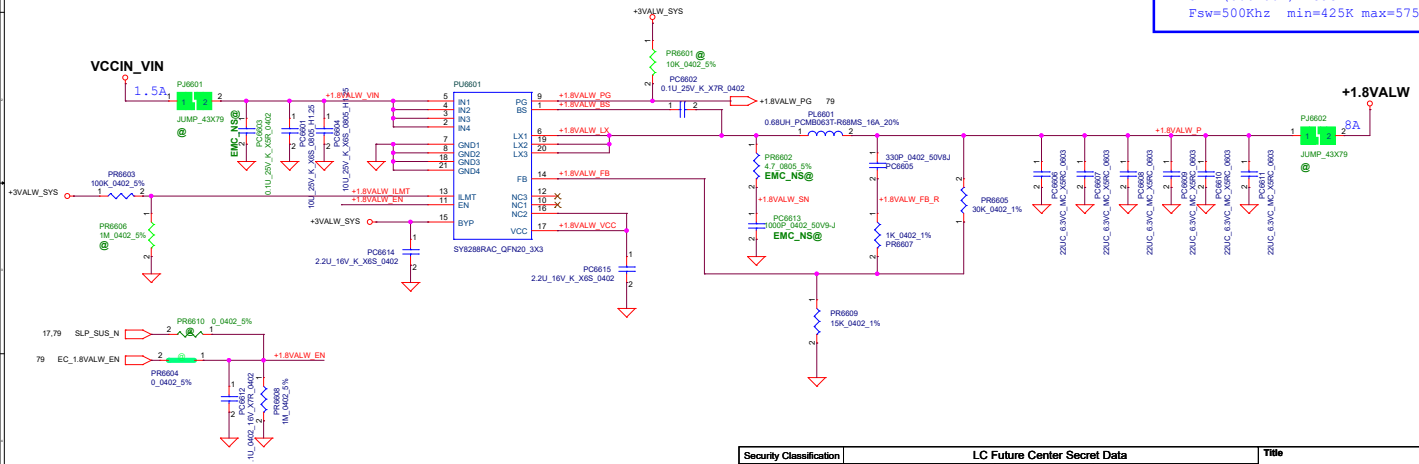



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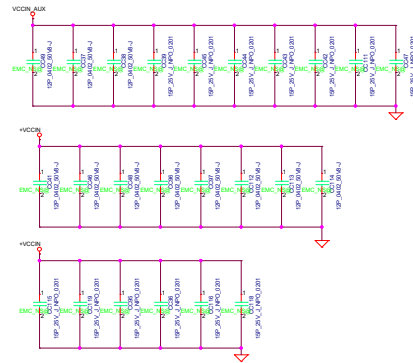
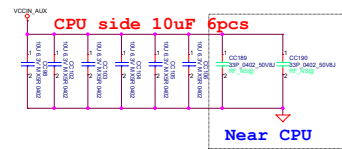
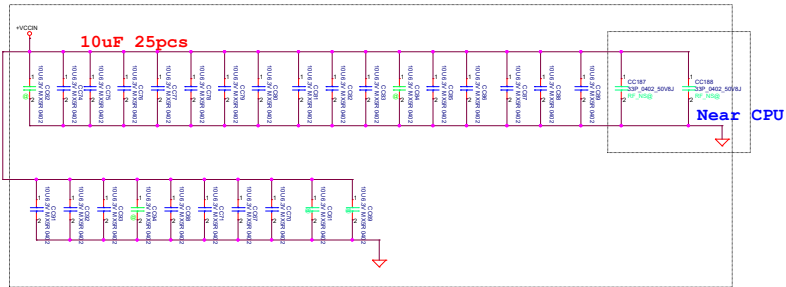




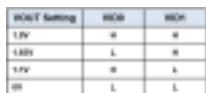
$V_{out}=1.8V\pm5\%$   
 $V_{set}=1.8V\pm2.3\%$   
 $V_{ref}=0.6V(+1\%)$   
 $TDC=8A$   
 $OCP=16A$   
 $OVP=(1.15-1.25)*V_{out}$   
 $UVP=(0.6-0.7)*V_{out}$   
 $F_{sw}=500Khz$  min=425K max=575K



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Date		Monday, March 29, 2021		Sheet 97 of 110	




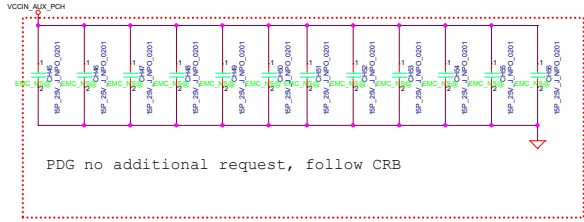
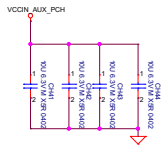
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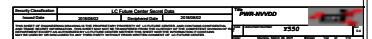
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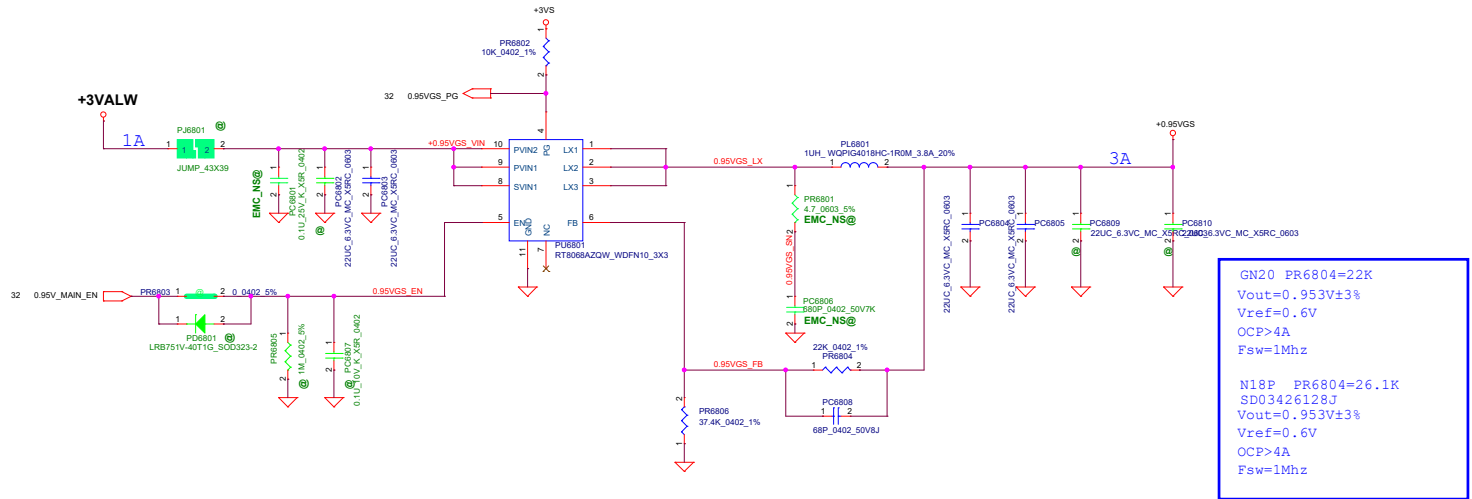


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